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GALLIUM ARSENIDE PILOT LINE FOR HIGH PERFORMANCE COMPONENTS

Contract No. F29601-87-C-0202

Semiannual Technical Report for September, 1989 through March, 1990

June 11, 1990

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DEFENSE ADVANCED RESEARCH PROJECTS AGENCY
DARPA/DSO
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GALLIUM ARSENIDE PILOT LINE FOR HIGH PERFORMANCE COMPONENTS

Semiannual Technical Report
April, 1990

1. INTRODUCTION (S. F. Nygren)

The Gallium Arsenide Pilot Line for High Performance Components (Pilot Line III) is to develop a facility for the fabrication of GaAs logic and memory chips. We have completed the first thirty-six months of this contract, and this report covers the period from September 25, 1989, through March 25, 1990. All the elements of this program are now in place. HCAD, our "User Friendly" CAD system, is complete; it was used to design two successful circuits - the Standard Cell Transversal Filter Chip (TFC) and the Cell Array Casino Test Chip. Our work with the 200 MHz, stepping-stone PT-2M memory is complete. The first wafers of 4K SRAM have recently been fabricated, and we have a design trick planned to enhance the 125°C operation of the second iteration of the 4K SRAM. The Custom ALU, Standard Cell TFC, Standard Cell ALU, and 1K Cell Array logic circuits all show similar performance. They satisfy the power supply, speed, and temperature design goals, but they don't comply with the I/O voltage requirements. We believe this is because we used preliminary models to design these circuits. While these circuits don't meet all their design goals, the current models accurately describe the way they perform. We therefore expect the final circuits, the ones designed with the latest models, to meet the design goals. These final circuits are now in wafer fab (4K SRAM, Cell Array Casino Test Chip) or in final layout (32-bit Multiplier). Unfortunately, progress has been slowed somewhat because of processing problems that occurred in photoresist developing, SiON dielectric deposition, and SiON etching. These problems caused delays in wafer processing; they also produced flawed wafers whose defects went undetected until they reached a process step where electrical measurements could be made.

With the addition of support for a 5K gate array, HCAD is now complete. The final version supports full custom, macrocell (standard cell), and gate array styles of layout. There are 45 elements in the macrocell library, and 30 elements in the gate array library. The gate array floorplan will support designs with up to 3500 used gates. To show the gate array capabilities of HCAD, we used it to personalize the Casino Test Chip function onto the array. This chip is now being fabricated. The macrocell capabilities were shown by designing the Transversal Filter Chip, a circuit whose initial masks produced fully functional devices. The custom capabilities were demonstrated previously.

We completed our work with the 256-bit PT-2M memory, our workhorse stepping stone toward the required 4K SRAM. As MBE and wafer processing improved so that FET characteristics approached the design targets, the yield and quality of PT-2M memories increased. The best result was achieved in two wafers from lot 33820 that had 9.2% and 3.5% yields, respectively, of chips that met all power supply, I/O voltage, and speed requirements at 40°C. Three wafer fab lots of 4K SRAMs have been completed to date, but they could not be tested for functionality because of processing problems involving vias and shorts.

We plan a redesign of the 4K SRAM after we have test data from the initial version. At 125°C, we expect the initial 4K SRAM will suffer from slow access times or pattern dependence due to subthreshold currents in the wordline access transistors. In the 4K SRAM redesign, we will solve this problem by using a diode to raise the memory array's negative power supply to about 0.5 V. Then the wordline access transistors can be biased to V_{gs} = -0.5 V, decreasing the subthreshold current by two orders of magnitude.

In logic circuits, we now have data from three full-sized demonstration circuits (Full-custom ALU, Standard Cell ALU, and Standard Cell Transversal Filter Chip), and a 1K Cell Array that is a stepping stone toward the full-size cell array demonstration circuit. All four of these were "right first time" designs; that is, the initial mask sets produced fully functional circuits. In general, these circuits operate properly and meet the specifications for power supply voltage, speed, and temperature: $V_{DD} = 2.0 \pm 10\%$, 200 MHz (normalized to 15 - 20 gate delays), -55 to 125°C. However, these circuits have difficulty complying with the specifications for I/O voltage levels and with meeting all specifications simultaneously. We believe this is because circuit design models, MBE structures, and wafer processing were evolving simultaneously. Consequently, these circuits were designed with models that have now been shown inadequate. In particular, the old models incorrectly simulated both the input switchpoint and the output-buffer voltage levels. The newer models simulate actual circuit performance much more closely. These newer models were used in the design of the 4K SRAM, Cell Array Casino Test Chip, and Full-custom 32-bit Multiplier. Both the 4K SRAM and Cell Array Casino Test Chip are currently in wafer fab, and we await completion of fabrication and confirmation of the new models. The 32-bit Multiplier will probably go to mask in early May.

We have now delivered eight sets of circuits to DARPA. The two most recent lots contained PT-2M memories in TriQuint PK-MLC-44-S packages, Full-custom ALUs in TriQuint PK-MLC 196-S packages, and 1K Cell Arrays in Interamics 64/88 packages.

During this reporting period, 241 MBE wafers were delivered to the wafer fabrication line under the Pilot Line III program, 233 wafers were started into wafer fabrication, and 165 wafers were completed and PCM tested. In comparison, during the previous reporting period there were 319 MBE wafers, 291 starts, and 238 completions. The reduced quantity of MBE wafers and starts in this period was partially due to a power failure that shut down the MBE machines and caused an unexpected 3-week interruption in the wafer supply. The reduced quantity of finishes was caused by the MBE problems in combination with wafer processing problems: first photoresist developing, then SiON dielectric deposition and etching. For the Pilot Line III program and other AT&T GaAs programs, total wafer fabrication starts averaged 33 per week. The wafer fabrication interval increased to 34 working days in March, 1990, compared to 28 working days in September, 1989. The increase is because of the equipment problems mentioned above.

We considerably increased the effort put into Statistical Process Control and a total quality management plan. There are now quality improvement teams for each process block (e.g., MBE, metals, photoresist). Virtually all operations have control charts in place, and we are working to insure that utility, not just quantity, of charts is increased. During this period, we decreased the number of out-of-range points from an average 25% to 5% on a weekly basis.

EFETs from the ED10 MBE structure have characteristics that center on the design target; DFETs have thresholds that average 60 mV too positive. We understand this as a failure of the MBE model, in that it did not account for the carbon at the substrate-layer interface. ED11 is a revised MBE structure that is free from interfacial carbon, has reduced sidegating, and is targeted to meet the design objective for FET characteristics. Preliminary data suggest ED11 met its objectives, but comprehensive data are not yet available because of the problems that arose in the MBE and processing areas.

We discovered that DFETs show good scaling behavior as device width is varied from 50 to 3 μm, but EFETs don't. This is a serious problem that affects the performance of all our circuits, because device currents for small devices won't be what the designers intended. So far we have determined that EFET scaling is better when EFETs are formed on a planar surface rather than in tubs. This problem is being actively investigated.

Except for reliability studies, we completed our investigation of the manufacturing feasibility of an Advanced Technology. The full Advanced Technology uses aluminum interconnect metallization rather than gold, 1.5 μm lines and spaces rather than 2.0 μm, and an improved implementation of the SFFL logic gate. We studied this technology in two parallel efforts. We developed the aluminum metal process using 1) WSi as a barrier between the gold-based ohmic contacts and the aluminum interconnects and 2) using sidewalls on gate and bottom metals to prevent aluminum stringers. We also demonstrated a planarization process to prevent problems in delineating topmetal, although we have not yet integrated planarization into the whole process. Without planarization, the aluminum process has superior via yields compared to gold, but poorer crossover and serpentine yields. With planarization, we expect comparable yields.

In parallel, we demonstrated Advanced Technology circuit performance using gold metallization with 1.5 μm lines and spaces. The PT-2L Standard Cell Multiplier was redesigned for the Advanced Technology. It operated under 100 ps/gate, easily meeting the 400 MHz speed requirement. Overall, the dc functional yield of these Advanced Technology multipliers was as high as 60% of the baseline Technology yield. That is, the 1.5 μm rules reduced the yield by 10%, and the actual circuit yields were 67% of Baseline circuits. When the Baseline Technology reaches a 10% yield, the Advanced Technology will reach a 6% yield, twice the 3% objective.

Radiation hardness studies on the Advanced Technology produced total dose results comparable to the Baseline Technology, but transient ionizing dose results inferior to the Baseline Technology. For total dose, exposure to $1\text{x}10^8$ rad(GaAs) gamma radiation from Co^{60} reduced EFET and DFET thresholds by 18 mV and 22 mV, respectively; ring oscillator frequency decreased by 10%. For transient dose, ring oscillators stopped oscillating at dose rates about $5\text{x}10^8$ rad(GaAs)/sec, with recovery times in the millisecond range. Baseline Technology ring oscillators worked until about $5\text{x}10^9$ rad(GaAs)/sec, and then recovered in less than 50 ns.

In the Baseline Technology, the PT-2M memory was tested for Single Event Upset using heavy ions. The LET threshold was about 0.2 MeV$*$cm^2/mg and 0.35 MeV$*$cm^2/mg for the standard and rad hard designs, respectively. At a LET value of 44 MeV$*$cm^2/mg, using Ni, the upset cross-sections per cell were about $2.25\text{x}10^{-6}$ cm^2 and $1.22\text{x}10^{-6}$ cm^2.

Reliability testing of the PT-2M memory is underway. For thermal aging, after 1000 hours, no significant changes or trends are seen at 150, 175, or 200°C. For high temperature operating bias, no significant changes have occurred after 64 hours at 150, 175, or 200°C. Both results suggest good stability to thermal effects.

2. HCAD: A User Friendly CAD System (L. Fisher, M. Nguyen)

The sixth half year of the program saw the HCAD efforts change from development-oriented to support- and maintenance-oriented, with the exception of developing support for the 5K gate array.

The first release of HCAD was delivered to AT&T at the end of October, 1989, and included full support for the Pilot Line with the exception of the 5K gate array floorplan which was then still under development.

An additional release of HCAD, completed recently, adds support for the 5K gate array floorplan and includes bug fixes and enhancements to existing capabilities.

The current version fully supports full custom, macrocell and gate array styles of layout. A macrocell library with over 45 elements is included, as is a gate array library with 30 elements. The gate array floorplan included will support designs with up to 3,500 used gates. Table 1 lists the elements in the cell library, and Table 2 lists the elements in the gate array library.

Table 1 — SUMMARY OF HCAD MACROFUNCTION LIBRARY

Cell Name	Function	layout	symbol	gate schematic	circuit schematic
aoi3333	and-or-invert	yes	yes	yes	yes
barsrb4	barrel shifter	yes	yes	yes	yes
bclab4	adder	yes	yes	yes	yes
bme	multiplier/encoder	yes	yes	yes	yes
bmfab4	booth multiplier	yes	yes	yes	yes
bmhab4	booth multiplier	yes	yes	yes	yes
bmmuxb4	booth multiplier	yes	yes	yes	yes
ckdrv_m	clock driver	yes	yes	yes	yes
clab4	adder	yes	yes	yes	yes
clcb4	carry lookahead	yes	yes	yes	yes
ctrdb4	down counter	yes	yes	yes	yes
ctrdpb4	down counter	yes	yes	yes	yes
ctrub4	up counter	yes	yes	yes	yes
ctrudb4	up/down counter	yes	yes	yes	yes
ctrudpb4	up/down counter	yes	yes	yes	yes
ctrupb4	up counter	yes	yes	yes	yes
daoi22	dual and-or-invert	yes	yes	yes	yes
daoi32	dual and-or-invert	yes	yes	yes	yes
daoi33	dual and-or-invert	yes	yes	yes	yes
decb4	decoder	yes	yes	yes	yes
dinrb	dual inverter	yes	yes	yes	yes
dmux	dual multiplexor	yes	yes	yes	yes
dnr2	dual nor	yes	yes	yes	yes
dnr3	dual nor	yes	yes	yes	yes
dnr4	dual nor	yes	yes	yes	yes
dnr5	dual nor	yes	yes	yes	yes
dxnor	dual exclusive nor	yes	yes	yes	yes
dxor	dual exclusive nor	yes	yes	yes	yes
fadd	adder	yes	yes	yes	yes
fd1s2ax_m	flip-flop	yes	yes	yes	yes
fd1s2dx_m	flip-flop	yes	yes	yes	yes
fd1s2nx_m	flip-flop	yes	yes	yes	yes
fd1s5f_m	flip-flop	yes	yes	yes	yes
hadd	adder	yes	yes	yes	yes
regfb44	register file	yes	yes	yes	yes
scanrfb4	register file	yes	yes	yes	yes
sdatemplate	unspecified	yes	yes	yes	yes
sigdrv_m	driver	yes	yes	yes	yes
srmxpib4	shift register	yes	yes	yes	yes
srpipob4	shift register	yes	yes	yes	yes
srpisob4	shift register	yes	yes	yes	yes
srrfb4	shift register	yes	yes	yes	yes
srsipob4	shift register	yes	yes	yes	yes
tbfin_m	tri-state buffer	yes	yes	yes	yes

Table 2 — SUMMARY OF HCAD GATE ARRAY LIBRARY

Cell Name	Function	layout	symbol	gate schematic	circuit schematic
ninrb	low drive inverter	yes	yes	yes	yes
minrb	medium drive inverter	yes	yes	yes	yes
hinrb	high drive inverter	yes	yes	yes	yes
nnr2	low drive nor2	yes	yes	yes	yes
mnr2	medium drive nor2	yes	yes	yes	yes
hnr2	high drive nor2	yes	yes	yes	yes
nnr3	low drive nor3	yes	yes	yes	yes
mnr3	medium drive nor3	yes	yes	yes	yes
hnr3	high drive nor3	yes	yes	yes	yes
nnr4	low drive nor4	yes	yes	yes	yes
mnr4	medium drive nor4	yes	yes	yes	yes
hnr4	high drive nor4	yes	yes	yes	yes
nnr5	low drive nor5	yes	yes	yes	yes
mnr5	medium drive nor5	yes	yes	yes	yes
hnr5	high drive nor5	yes	yes	yes	yes
nmux21	low drive 2-to-1 mux	yes	yes	yes	yes
mmux21	medium drive 2-to-1 mux	yes	yes	yes	yes
hmux21	high drive 2-to-1 mux	yes	yes	yes	yes
noai22	low drive or-and-invert	yes	yes	yes	yes
moai22	medium drive or-and-invert	yes	yes	yes	yes
hoai22	high drive or-and-invert	yes	yes	yes	yes
nfd1s2ax	low drive flip-flop	yes	yes	yes	yes
mfd1s2ax	medium drive flip-flop	yes	yes	yes	yes
hfd1s2ax	high drive flip-flop	yes	yes	yes	yes
ckdrv	clock driver	yes	yes	yes	yes
sigdrv	signal driver	yes	yes	yes	yes
mca50rlp	output pad	yes	yes	yes	yes
mca50tbp	output pad	yes	yes	yes	yes
mcainrlp	input pad	yes	yes	yes	yes
mcaintbp	input pad	yes	yes	yes	yes

The standard cell capabilities of HCAD have been well exercised by the designers of the Transversal Filter Chip. The full custom capabilities of HCAD have been exercised by the HCAD developers (setting up the standard cell library) and independently by designers at the Hughes Microelectronics Center. The Gate Array tools and their integration have been exercised during the design and layout of the gate array Casino Test Chip.

The AT&T HCAD macrocell library has been extensively checked, including design rule checks, device level extraction and layout-to-logic verification, logic simulation, fault simulation, and timing simulation. The gate array library has also been checked.

The Hughes TEST (HTEST) tools are integrated into HCAD. These tools support the design of chips that include testability enhancing features such as set scan registers. Elements in the macrocell library have been designed to support a scan design methodology.

A set of model parameters are included that support of HSPICE, the circuit-level simulator in HCAD. Six sets of parameters are provided: two temperatures (25°C and 125°C), each with three process conditions (nominal, fast, and slow). In addition, the HSPICE interface provides a "macro model" capability, allowing the inclusion of a gate resistance term in the model.

The technology files in HCAD have been updated as necessary to track new developments and changes in the Pilot Line III technology and to provide additional functionality.

HCAD is built within the Design Framework provided by Cadence. This Framework has allowed a full-featured design system to be provided in support of the DARPA AT&T Pilot Line III. Table 3 highlights some of the key features of HCAD and indicates which tools are used.

Table 3 — SUMMARY OF HCAD CAPABILITIES AND TOOLS

Function	Tool
CAD Framework	Cadence Design Framework
Schematic Editor	Cadence Schematic Editor
Logic Simulation	SILOS
Fault Simulation	SILOS
Test Vector Generation	HITS
Behavior/Functional Simulation	Zycad/Endot N.2
Gate Array Place and Route	Mentor GateStation
Std. Cell Place and Route	Cadence StandardEdge
Full-Custom Layout	Cadence Graphics Editor
Static Timing Analysis	Cadence TA
Post Layout Simulation	SILOS, TA, HSPICE
Circuit Simulation	HSPICE
Layout Verification	Cadence PDCheck, PDExtract, PDCompare
Design-For-Test	Hughes HTEST

CAD technology, just like process technology, does not stand still. Thus, there is room for improvement of HCAD. The vendors of the tools used in HCAD are presently releasing new tools that:

- Add support for VHDL - the DoD mandated hardware description language.
- Add support for symbolic layout and compaction.
- Add support for logic synthesis and optimization.
- Improve the performance, quality, and density of standard cell (macrocell) designs.

Even though HCAD has now been released (and is no longer under active development), the users of HCAD will be able to continue to receive enhancements to their tools through the efforts of the commercial tool vendors.

3. DEMONSTRATION VEHICLES

3.1 Circuit Overview (C. H. Tzinis, S. F. Nygren)

This contract requires SRAM, Custom Logic, Standard Cell Logic, and Cell Array Logic circuits that operate at a 200 MHz clock over -55 to 125°C. To achieve this goal, we designed five sets of small scale circuits (PT-0, PT-1, PT-2L, PT-2M, and 1K Cell Array) plus eight full size circuits, as shown in Table 4.

Table 4 — CIRCUITS DESIGNED FOR PILOT LINE III

	Style	Size	Status
PT-0	Custom	FETs Only	Work Complete
PT-1	Various Various	Small Logic Unclocked 256-bit SRAM	Work Complete Work Complete
PT-2L	Various	364-2211 Logic Gates	Work Complete
PT-2M	Various Custom	91-283 Logic Gates Clocked 256-bit SRAM	Work Complete Active Effort
1K Cell Array	Cell Array	738 Logic Gates	Active Effort
4K SRAM	Custom	4096-bit SRAM	Initial Testing
4K SRAM II	Custom	4096-bit SRAM	Planned
32-bit Multiplier	Custom	6500 Logic Gates	In Design
ALU	Custom	3571 Logic Gates	Active Effort
ALU	Std. Cell	3452 Logic Gates	Active Effort
Transversal Filter	Std. Cell	5190 Logic Gates	Active Effort
Casino Test Chip	Std. Cell	3700 Logic Gates	Work Complete
Casino Test Chip	Cell Array	4126 Logic Gates	In Wafer Fab

A rigorous evaluation of each circuit would consider five criteria:

Functionality	Logic: pass all test vectors at 25°C Memory: all bits work at 25°C
V_{DD}	Works for $1.8 < V_{DD} < 2.2$V
I/O	Complies with all I/O voltage specifications ($V_{ih} \leq 0.9$, $V_{il} \geq 0.3$, $V_{oh} \geq 1.0$, $V_{ol} \leq 0.2$V
Speed	Logic: works at 200 MHz for 15-20 gate delays Memory: works at 200 MHz
Temperature	Works from -55 to 125°C

The best results for the presently active circuits are shown in Table 5. For some circuits, more than one example is given.

Table 5 — BEST CIRCUIT RESULTS

Memory	
• PT-2M	— Satisfies functionality, V_{DD}, I/O, and speed for 0-80°C — Satisfies functionality, I/O, and temperature at 50 MHz over part of the V_{DD} range.
Custom	
• ALU	— Satisfies functionality, speed, and temperature at V_{DD} = 2.0V, but fails one of the four I/O specifications. — Satisfies functionality, V_{DD}, and speed over 25-125°C, but fails one of four I/O specifications.
Standard Cell	
• ALU	— Satisfies functionality, V_{DD}, and I/O at 100 MHz and 25°C
• Transversal Filter	— Satisfies functionality at V_{DD} = 1.9V, but fails one of the four I/O specifications; no speed or temperature measurements performed
Cell Array	
• 1K Cell Array	— Satisfies functionality, V_{DD}, and I/O at 100 MHz and 25°C — Satisfies functionality, speed, and temperature at 2.2V, but fails one of the four I/O specifications.

As Table 5 shows, we have demonstrated circuits that meet the speed and temperature requirements of the program. However, we have not demonstrated a circuit that completely complies with all evaluation criteria. Part of this problem is that circuit design models have been evolving simultaneous with circuit design and fabrication. All the circuits described in Table 5 were designed using circuit models known as SargicS.11. We previously described that this model incorrectly models input switch points: the measured values are about 250 mV higher than the model predicted. Similarly, the output levels are incorrectly modeled (see Section 3.5 for a further discussion of this). New models (SargicS.15) have been used to design the 4K SRAM, the 32-bit Multiplier, and the Cell Array Casino Test Chip. We anticipate that these circuits will come much closer to meeting all design specifications.

3.2 PT-2M and 4K SRAM Memory Test Results (W. R. Ortner)

PT-2M Wafer Test Results

Twenty one PT-2M wafers from four lots have been tested during the current six month period. There were no working chips in lot 34430. As shown in Table 6, all other wafers have working chips. Two wafers from lot 33820 have significant Bin 1† yield (9.2% and 3.5%).

PT-2M Package Test Results

In each of the last four quarters, we delivered to DARPA 20 of the best PT-2M devices available at that time. While all the delivered devices meet some of the requirements, March, 1990, is the first time all 20 devices met all requirements at 25°C.

PT-2M Package Results (Deliverables)					
	Number of Bin 1's Delivered†				
	125°C	80°C	25°C	0°C	-55°C
Jun '89	0	0	0	0	0
Sep '89	0	2	0	0	0
Dec '89	0	3	5	1	0
Mar '90	0	1	20	8	0

4K SRAM I

The 4K SRAM I wafer test program, fixturing, and probe card are ready and have been used to test the third 4K lot. The first two 4K lots had poor PCM parametric yield and were rejected prior to wafer test. The third lot 34540 also has very poor PCM yield, but it served as a vehicle to debug the program, fixturing, and probe card. All six wafers have "shorts" and "contact" problems, very low I_{dd} and I_{dds} currents and no working bits. The "shorts" are on V_{DD} and to a lesser extent on V_{ddq} (output circuit power). Preliminary results indicate that these problems are due to wafer processing mishaps rather than circuit design flaws.

PT-2M DEVICE PERFORMANCE vs. FET CHARACTERISTICS

EFET and DFET data from PCM sites are joined with PT-2M test results to characterize memory performance as a function of FET parameters. In Figures 1 and 2 the EFET and DFET saturation current (I_{ds}) and the threshold voltage (V_{th}) are scatter plotted for functional yield levels ranging up to ≥50%. In each figure, a small rectangle shows the design target for I_{ds} and V_{th}. As FET characteristics approach the design window, yield increases. Greater than 50% yield is achieved when EFETs have I_{ds} = 40 mA/mm and V_{th} = 260 mV, and DFETs have I_{ds} = 100 mA/mm and V_{th} = 550 mV.

In Figure 3, the E/D current ratio is scattered plotted against Functional Yield and Ripple Mode Access Time. A smooth fit curve is shown. Both parameters are optimized at an E/D current ratio of 0.4.

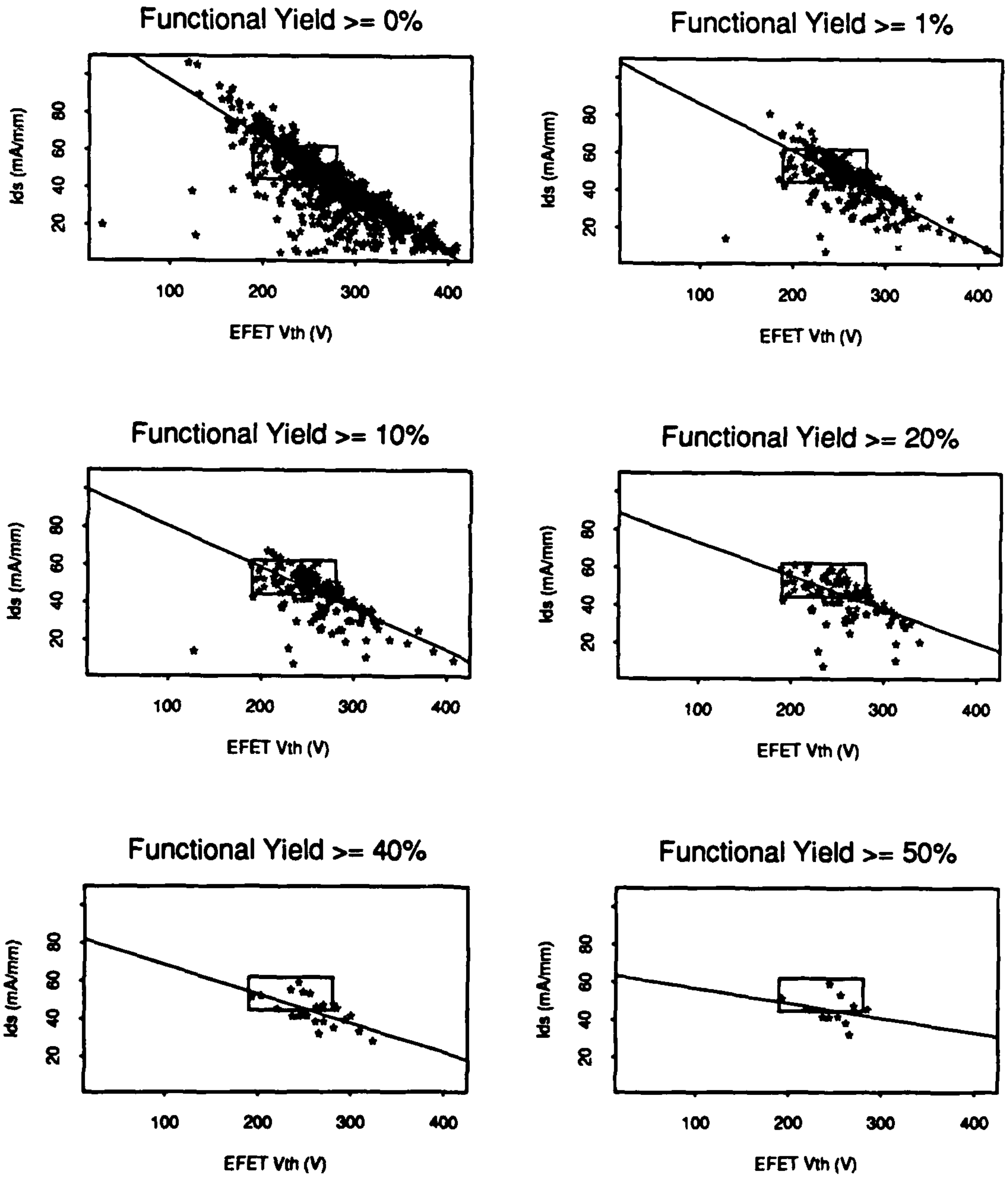
---

† Bin 1 Devices Meet all Requirements at 200MHz

Table 6 — PT-2M WAFER TEST RESULTS - OCT '89 THRU MAR '90

Wafer	°C	Meet Design Goals			
		Work	Power Supply	I/O Levels	Speed
33611	40	33	6	0	0
33612	40	51	13	0	0
33613	40	78	57	0	0
33614	40	38	26	0	0
33615	40	17	10	0	0
33616	40	61	42	1	1
33722	40	27	6	4	0
33723	40	15	1	1	0
33724	40	11	2	1	0
33725	40	67	25	18	0
33726	40	101	54	35	0
33823	40	174	161	130	50
33823	80	112	85	43	0
33823	100	47	33	9	0
33824	40	181	143	125	19
33824	80	191	166	111	3
33824	100	109	88	37	0
33824	120	95	81	1	0
33825	40	118	47	17	0
33825	80	60	14	0	0
33825	100	18	5	0	0
33825	120	7	2	0	0
33826	40	156	90	56	0
33826	80	54	17	1	0
33826	100	20	4	0	0
33826	120	2	0	0	0
34431	40	0	0	0	0
34432	40	0	0	0	0
34433	40	0	0	0	0
34434	40	0	0	0	0
34435	40	3	0	0	0
34436	40	0	0	0	0

1 There are 543 chips per wafer.
2 Work - at some V_{DD} (1.8V to 2.2V), V_{in} (0V to 1.2V) and V_{out} .6V .
3 Power Supply - Work over entire V_{DD} Power Supply Range at the above V_{in} V_{out} Levels.
4 I/O Levels - Work over entire V_{DD} Range, V_{ih} (.3 to .9) and V_{out} (.2 to 1.0).
5 Speed - Meet all Requirements at 200 MHz (i.e. Bin 1 Devices).



Functional Yield >= 0%

Functional Yield >= 1%

Functional Yield >= 10%

Functional Yield >= 20%

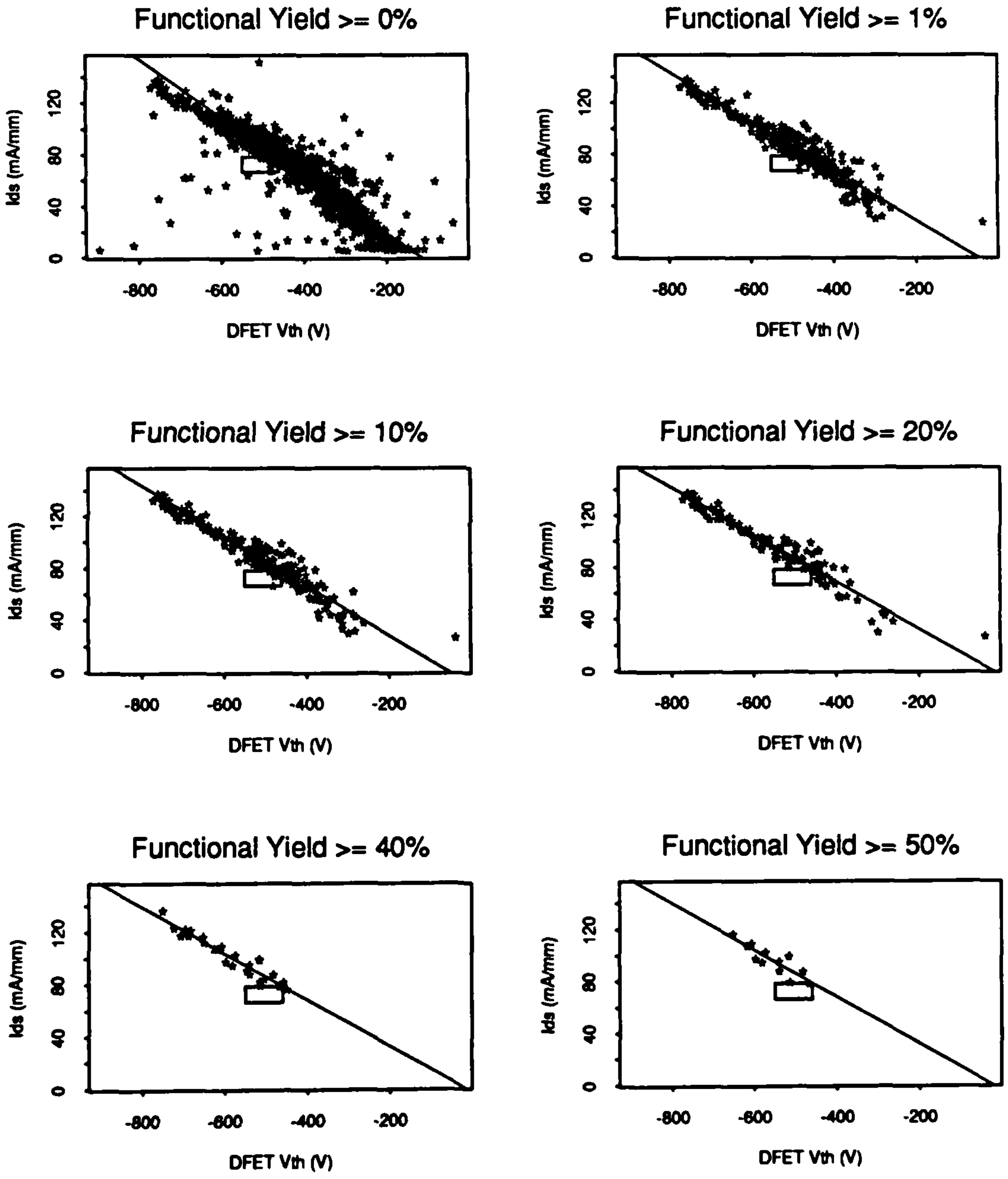
Functional Yield >= 40%

Functional Yield >= 50%

Boxed Area is sargic.11 Model Values Used to Design PT-2M

EFET Characteristics vs. PT-2M Yield

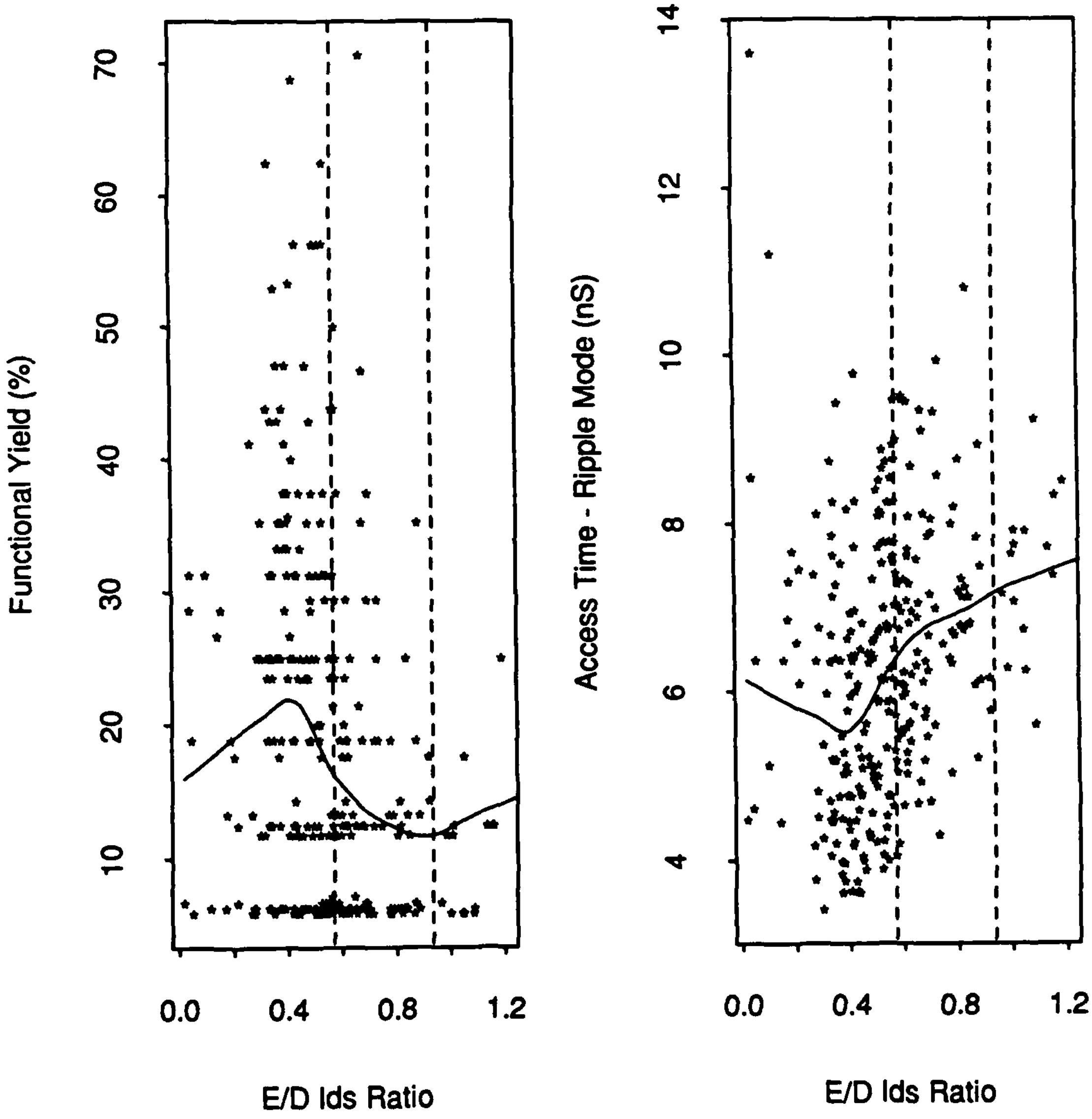
Figure 1.



Boxed Area is sargic.11 Model Values Used to Design PT-2M

DFET Characteristics vs. PT-2M Yield

Figure 2.



Dashed lines are the sargic.11 model extremes used to design PT-2M

E/D Ids Ratio vs. PT-2M Yield and Access Time

Figure 3.

3.3 SRAM II Memory Design (W. E. Werner)

A major concern in the 4K SRAM I design was the subthreshold leakage current in the 3µm wide EFETs. These devices are used in the memory cell as wordline access transistors. Early studies on these devices showed excess leakage current even with the gate to source negatively biased ($V_{gs} < 0$). After changes were made in wafer processing, the devices were again characterized. Recent data shows no excess current; the 3µm EFETs now look more like scaled versions of the 18µm EFET model. This means that a negative gate to source voltage will now greatly reduce the magnitude of subthreshold leakage current.

The 4K SRAM I operates with a bias voltage of $V_{gs} = -0.05$ volts on the wordline access transistor in the non-selected state. Simulations indicate that at high temperature (125°C), the magnitude of subthreshold leakage in the wordline access transistor will still be large enough to cause push out in access time or a pattern sensitivity in the memory array.

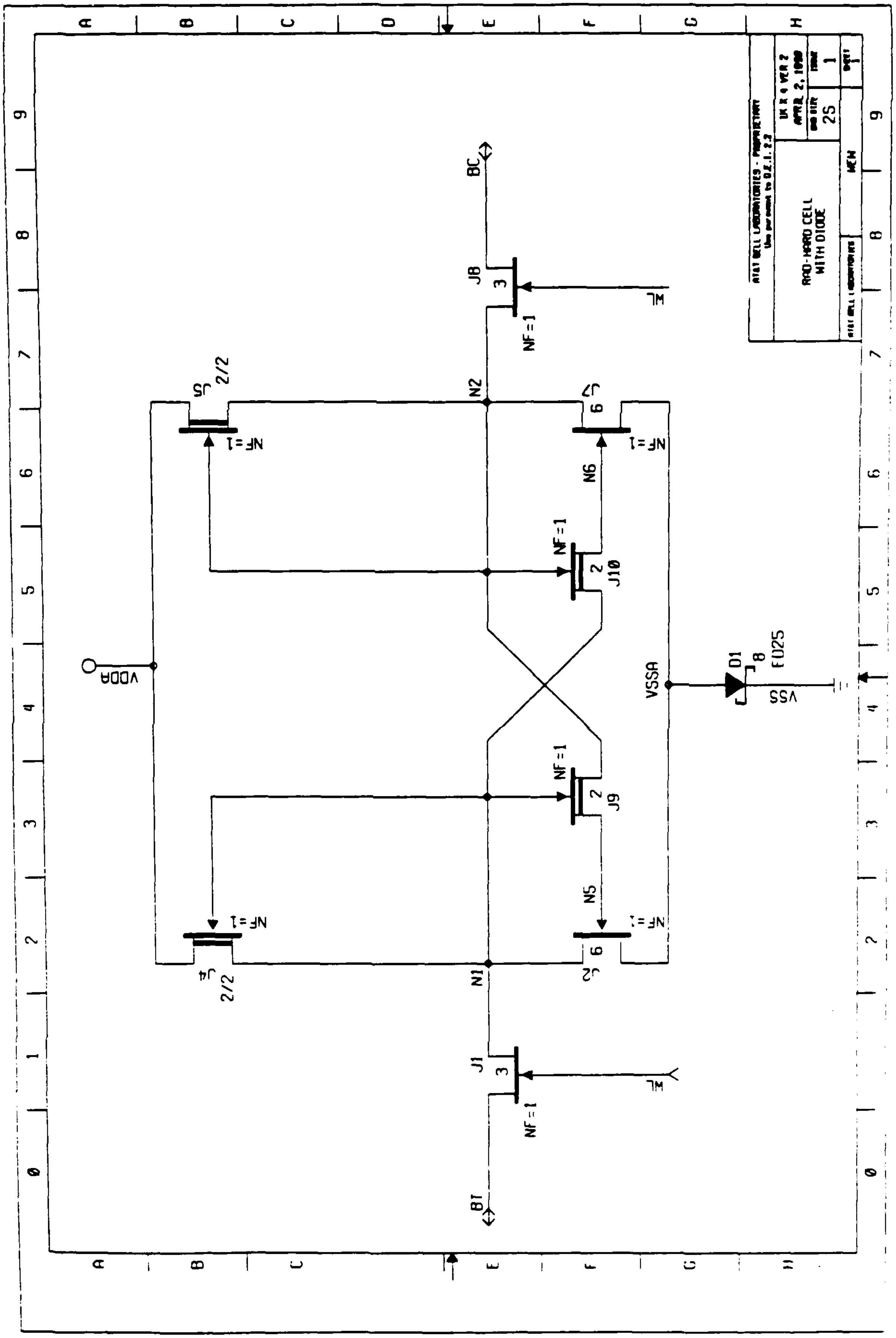
The 4K SRAM II design directly addresses this problem. Figure 4 shows the new memory cell. Diode D1 raises the array's negative power supply V_{SSA} to around 0.5 volts. The redesign of the memory cells allows the wordline access transistors J1 and J8 to be biased with $V_{gs} = -0.5$ volts. This negative bias will decrease the subthreshold leakage current by around two orders of magnitude.

Several other circuit changes were needed on the 4K SRAM II in order to properly interface with the new cell array design. Changes include the wordline driver, sense amplifier, level shifter, write select, column decoder and data-in latch.

Adding the diode to the cell and modifying other circuits increased the size of the layout. The cell array size was then reduced by replacing the four 2 x 1µm DFETs with two 2 x 2µm DFETs. This restored the layout to the same die size and bonding pad configuration as the 4K SRAM I.

The entire 4K SRAM II design has been simulated using ADVICE. The simulation conditions include all the modeled process extremes at 25°C and 125°C. In all cases the simulation results show that the circuits work properly. Even at high temperature and low EFET threshold conditions, no sign of access time push out or pattern sensitivity were observed.

We are presently waiting for test results from 4K SRAM I. If any inadequacies are found in the 4K SRAM I design that have not been predicted, there will be time to make the necessary circuit modifications in the 4K SRAM II design before its scheduled mask shop date.


BT
BC
J1
J8
3
NF=1
WL
N1
N2
J4
2/2
J5
2/2
J2
J7
6
N5
N6
J9
J10
2
VDDA
VSSA
D1
8
FD25
VSS
RAD-HARD CELL
WITH DIODE
AT&T BELL LABORATORIES - PROPRIETARY
APRIL 2, 1990
25
1
A
B
C
D
E
F
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0
1
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4
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7
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9

Radiation Hardened Cell with Diode

Figure 4.

3.4 Laser Programming (R. T. Smith, F. Fischer)

The main objectives during this reporting period were to establish and verify laser programming of Version I of the 4K SRAMs. Although all software was successfully developed and debugged, none of the first three 4K SRAM wafer lots yielded repairable chips, preventing demonstration of the complete process.

Laser link coordinates were acquired from the design team in October and used to generate appropriate off-line auxiliary files on the VAX 11/750 host computer in November. These files were used to verify the link coordinates and debug the downloading software to the ESI 8000 laser programming system in December, a few days ahead of schedule. In January and February, although the first 4K wafers were not viable for test purposes, they were used to evaluate and reject a proposed modification to the laser window etch process. These early wafers were also used to swap out rows and columns on the 4K SRAMs by February 20. However, because the wafers had poor parametric quality and zero functional or repairable yield, electrical verification of the laser programming operation was not possible in this reporting period.

3.5 1K Cell Array Test Results (C. H. Tzinis, L. Ackner, J. Scorzelli, R. J. Niescier, W. I. Satre)

The 1K Cell Array circuit is a stepping stone toward the Cell Array Casino Test Chip. During the period from October, 1989, through March, 1990, two lots were completed and tested. Testing for functionality at the wafer level was done on the Advantest T3340, whereas the packaged circuits were tested from -55°C to 125°C up to 200 MHz on the HP 82000. The wafer test results for lots 33730 and 34030 are summarized in Table 7. The PCM rating reflects how many sites out of the total number tested (16 per wafer) simultaneously fulfills EFET and DFET currents, and via resistance requirements (see Section 4.4 for details).

Table 7 — 1K CELL ARRAY WAFER YIELD SUMMARY

Lot Number	Functional Sites	Total Sites	Functional Yield	PCM Rating
33730	135	498	27%	54/96 = 56%
34030	40	415	10%	3/80 = 4%

Not all functional sites satisfy the I/O requirements. The primary failure mechanism is high V_{ih}, which was expected as the 1K Cell Array was designed with SargicS.11, a model that makes a 250 mV error in predicting the input switchpoint (see Section 3.1). However, data analysis revealed much higher V_{ih} than expected, prompting detailed investigation. We found holes in the shmoo plots which invalidated our search algorithm for testing. We used an improved search algorithm when we tested packaged devices. Figure 5 shows the I/O levels of 28 packaged devices in a boxplot format for -55, 25, and 125°C; each box contains the data for all three voltages -1.8, 2.0, and 2.2V. Next to the 25°C package data, the respective wafer probe data demonstrate the discrepancy in V_{ih}. The horizontal lines represent the specification levels, and it is apparent that the main failure mechanisms are V_{il} and V_{oh} at 125°C and marginal V_{ol}. Simulations with SargicS.15 predict the collapse of V_{oh} at 125°C, while the marginal V_{ol} is understood in terms of FET leakage around threshold voltage area (soft turn on). Figure 6 demonstrates the reduction of V_{oh} at 125°C as simulated by SargicS.15. The boxplots represent actual package data from Figure 5. Dotted lines show SargicS.15 models for this output buffer at 25°C (high, center, and low models: 25h, 25c, and 25l). Dashed lines show the three models at 125°C (125h, 125c, and 125l). The correlation with the measured results is apparent. Further analysis is continuing.

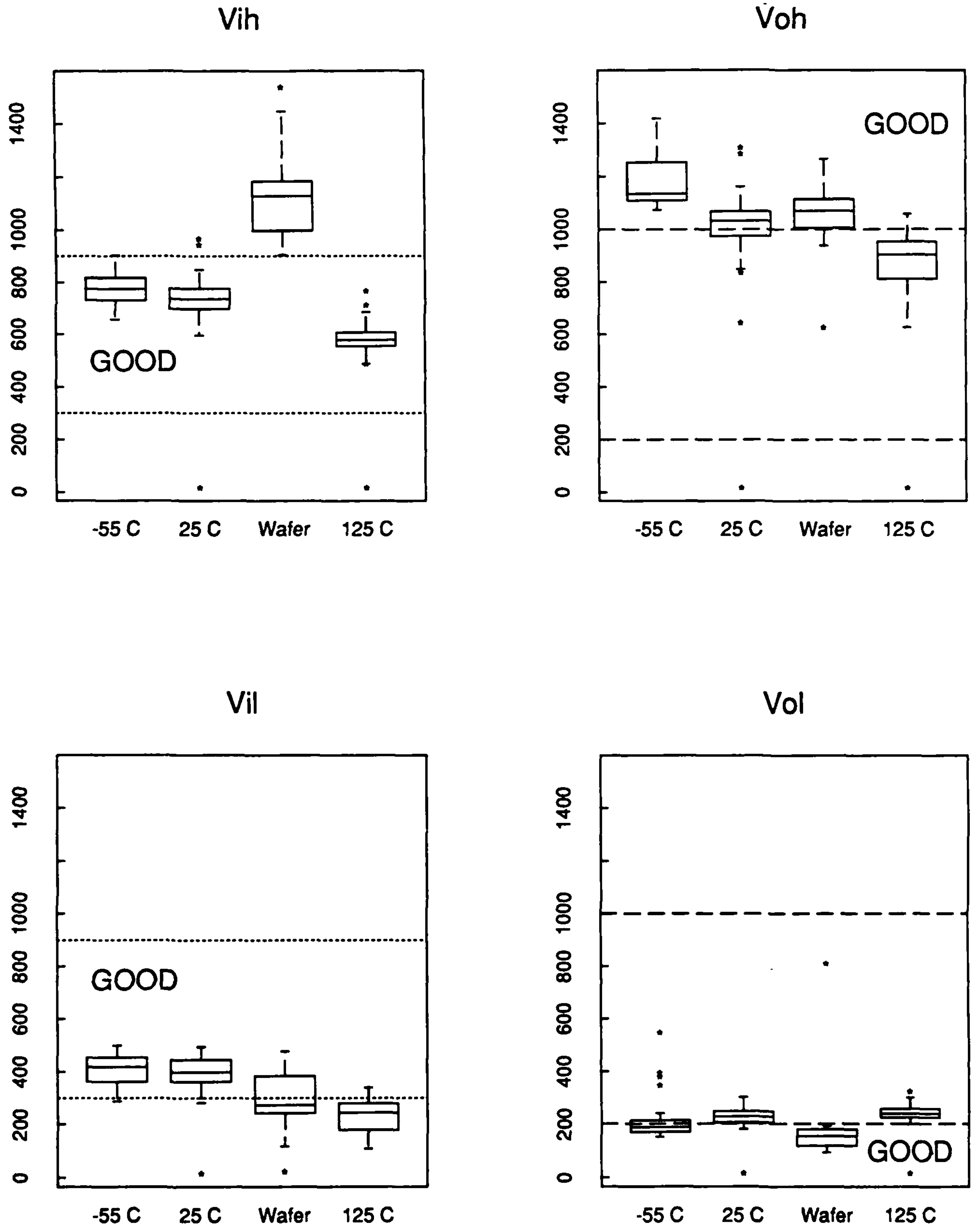
3.6 Custom ALU Test Results (C. H. Tzinis, L. Ackner)

The custom ALU is the oldest running code of the deliverable circuits, and nine lots have been completed and tested in the last six months. Four of them had no yield, as predicted from the PCM data. The data for the remaining five are summarized in Table 8.

Table 8 — CUSTOM ALU WAFER YIELD SUMMARY

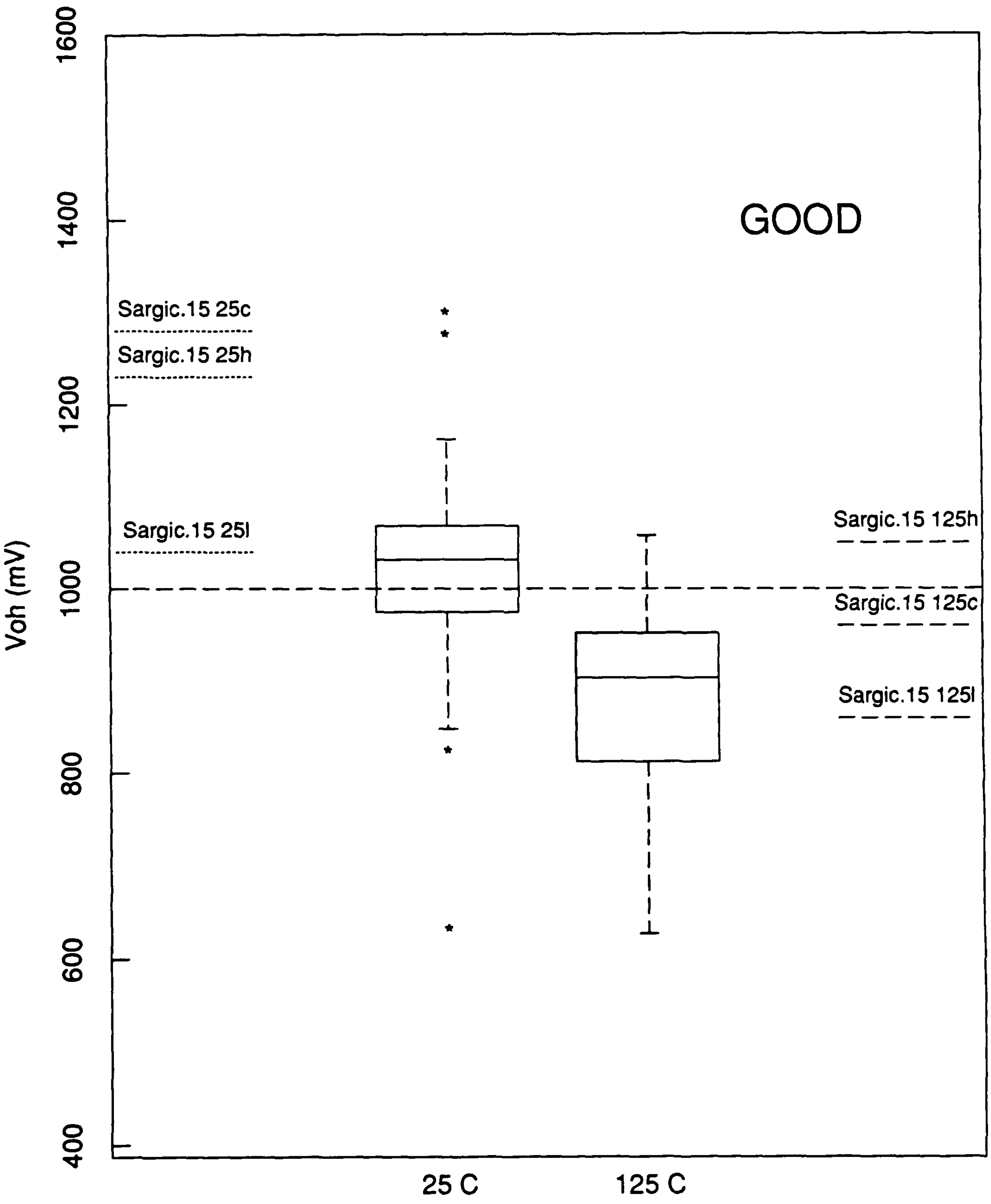
Lot Number	Functional Sites	Total Sites	Functional Yield	PCM Rating
33810	47	459	10%	8/144 = 6%
33970	11	255	4%	15/80 = 19%
34050	8	255	3%	11/80 = 14%
34340	1	204	0.5%	1/64 = 2%
34600	2	153	1%	1/48 = 2%

In the previous reporting period, we stated that wafer and package data did not match. We understand now that the first circuits had to operate at high V_{DD} which automatically increased the power dissipation by at least a factor of 2, subsequently raising the operating temperature to 70°C above room temperature. The present circuits dissipate an average 2.2W (vs. 2.7W simulated at 2.0V), operate in the 1.8V-2.2V range, and are tested at controlled temperatures. One surprising outcome of the investigation was the presence of holes in the shmoo plot of any I/O parameter vs. V_{DD}. This phenomenon is being investigated. Its immediate impact is demonstrated by irreproducible I/O level measurement; therefore, we currently read the I/O levels directly from the shmoo plot of the I/O voltage vs. V_{DD}. A possible culprit is sidegating, and our new MBE structure that suppresses sidegating is expected to alleviate the problem. Selected devices that were packaged for the December and March deliverables show that the primary failure mechanisms are low V_{oh} and



Wafer and Packaged Device I/O Levels for 1K Cell Array

Figure 5.



Comparison of Simulated and Measured V_{oh} for 1K Cell Array

Figure 6.

marginal V_{il} and V_{ol} (Figure 7). These observations are similar to the 1K Cell Array results and are mainly due to buffer design; the marginal V_{ol} is due to FET turn on characteristics.

3.7 Standard Cell ALU Test Results (C. H. Tzinis, L. Ackner)

The full-size Standard Cell ALU, a digital circuit with approximately 3,500 gate complexity, is one of the deliverable circuits specified in the contract. Circuit design was completed in July 1989 and three lots were completed in the period from October, 1989, to March, 1990. The test data for the non-zero yield lots are summarized in Table 9.

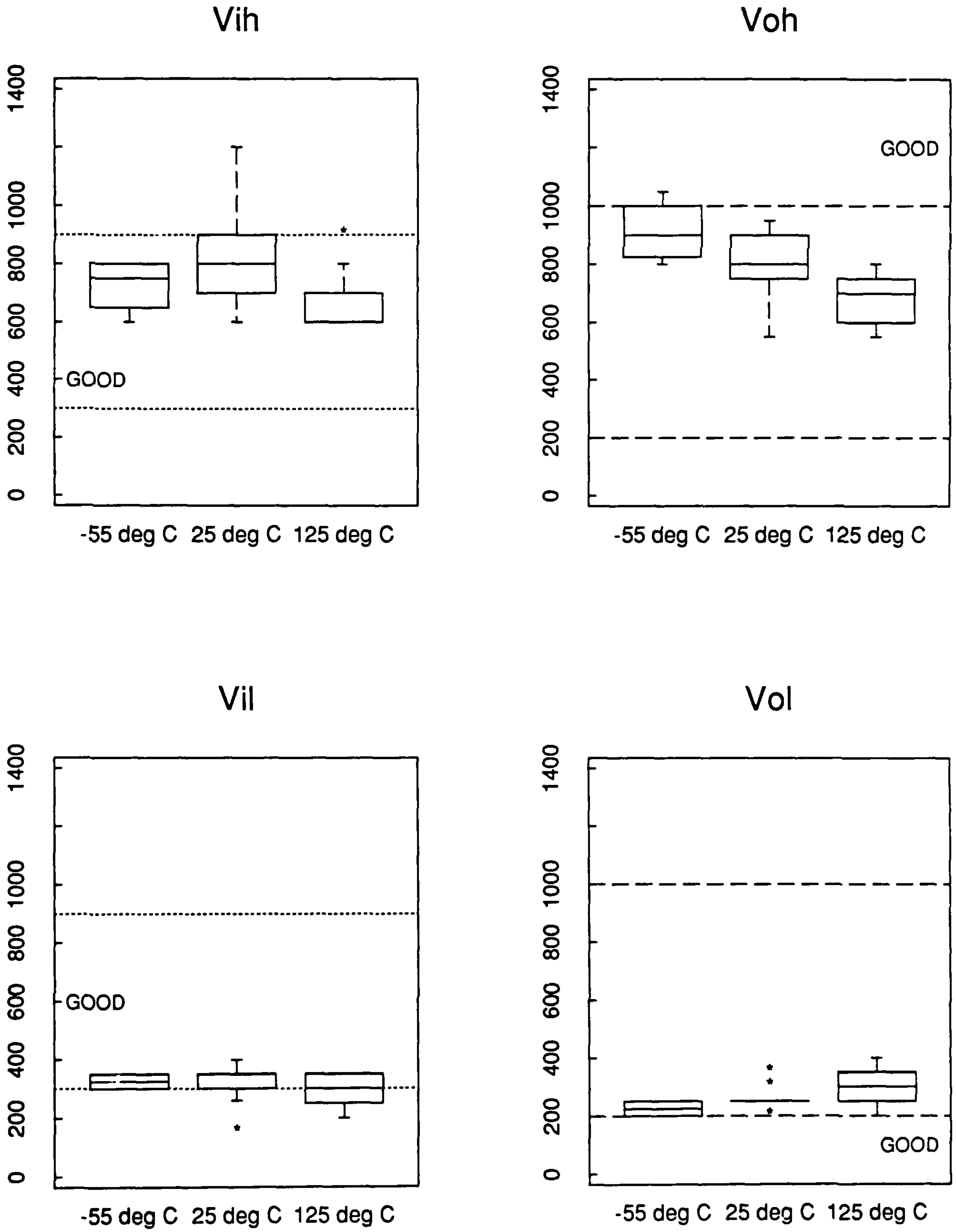
Table 9 — STANDARD CELL ALU WAFER YIELD SUMMARY

Lot Number	Functional Sites	Total Sites	Functional Yield	PCM Rating
33710	3	255	1%	27/101 = 27%
34060	5	306	2%	38/126 = 30%

Since the PCM Ratings are relatively high, the functional yield is disappointing. The devices from lot 33710 were marginal and operated in a very limited voltage area (V_{DD} = 2.7V); most of the devices of lot 34060 operated in nominal range. Three packages were tested and one of three devices satisfies all I/O requirements at room temperature and 100 MHz while another does so at -55°C and the same frequency. Higher operating frequencies are currently being tested. The average power dissipation is comparable to that of the custom ALU (2.1W at room temperature and 2.0V) (simulated power ~2.7W). In terms of design effort, the standard cell ALU required five staff-months to complete whereas the custom ALU took 24 staff-months. The standard cell design effort would have been somewhat longer, except it used the same logic design as the custom ALU and thereby benefited from the earlier custom design.

3.8 Standard Cell Transversal Filter Circuit Design and Test (S. W. White, E. K. Gee, W. T. Kuo)

The Transversal Filter Chip (TFC) contains 5.2K gates on a die which is approximately 360 mils per side. To date, five lots of Transversal Filter wafers have been processed, yielding two which passed PCM screening. These two were the first and third lots processed (33880 and 34140), and both were grown with the ED10 MBE structure. These two lots provided 11 wafers for wafer probe functional testing. Fully functional devices which passed all test vectors were found on both lots. As a result of this and the few testing problems that were encountered, extensive characterization of the functional and nearly functional circuits was possible. This analysis showed that most voltage levels met their specified values.



Packaged Device I/O Levels for Custom ALU

Figure 7.

As with the Standard Cell Casino Test Chip, Micro-Probe was contracted to deliver the TFC's 228-pin probe card. A 6-mil pad pitch was used on the TFC and there was no difficulty in manufacturing this card. Following delivery of the probe card, the test program and setup were debugged.

Initial wafer-probe testing began in November 1989 with delivery of Lot 33880. This lot contained 6 wafers of which two yielded a single fully functional part each. Lot 34140 containing 5 additional wafers was tested in December 1989 and yielded a single fully functional device. With 31 TFC sites per wafer, total yield is 3/341 (1%). Most wafer-probe testing was performed at 1 MHz although limited higher-speed testing up to 40 MHz yielded similar results.

The TFC's Ring Oscillator subcircuit was tested to better characterize the speed at which the TFC would run if not limited by tester capabilities. A high-bandwidth oscilloscope was used to probe the single oscillating output whose frequency is divided internally by a 16-stage ripple counter. To make optimal use of testing time, only the best performing devices (as measured by the functional test vectors) were probed. At V_{DD} = 2.0 V, the gate delays range from 193 ps to 294 ps, with the median delay being approximately 20% slower than simulated. (The contract speed requirement is 250-333 ps/gate.) The Ring Oscillator's layout was implemented in the same manner as the remainder of the circuit, using automatic placement and routing of standard cells. Given the realistic interconnects and dummy loads utilized in the oscillator's design, the legitimacy of its use as a vehicle for predicting the speed of the functional circuitry is ensured. As such, the predicted speed of TFC's from the two tested lots would be in the 130 MHz range. (There are 23 gates in the critical path.) This is the best estimate that can be made at this time without testing packaged parts at high-speed.

The median measured current drain at V_{DD} = 2.0 V is 2.54 A yielding a power dissipation of approximately 5.1 Watts. Of this, nearly 40% is dissipated solely by the output drivers. Excluding these drivers, the power dissipation translates into 0.66 mW per logic gate. Given that simulations predicted a total power dissipation of over 6 Watts, it is apparent that transistors on the tested wafers have lower current levels than predicted by the device models. This is consistent with the ring oscillator's measured delays being slower than simulated.

Output voltage levels were found to be superior to those of other circuits previously designed in this process. V_{ol} values were consistently under 75 mV while the specification requires that they be under 200 mV. Similarly, V_{oh} values were consistently over 1.25V while the specification requires that they be greater than 1.0 V. V_{il} levels also met the specification but not with the margin of the output voltages. V_{ih} and minimum V_{DD} voltages tended to be higher than their specified values of 900 mV and 1.8 V respectively. A summary of the voltage levels associated with the three fully functional TFCs appears in Table 10. Because of the excellent output levels, the measured I/O noise margins average in excess of 300 mV for both logic low and logic high values. As a result, these circuits would have no difficulty driving themselves.

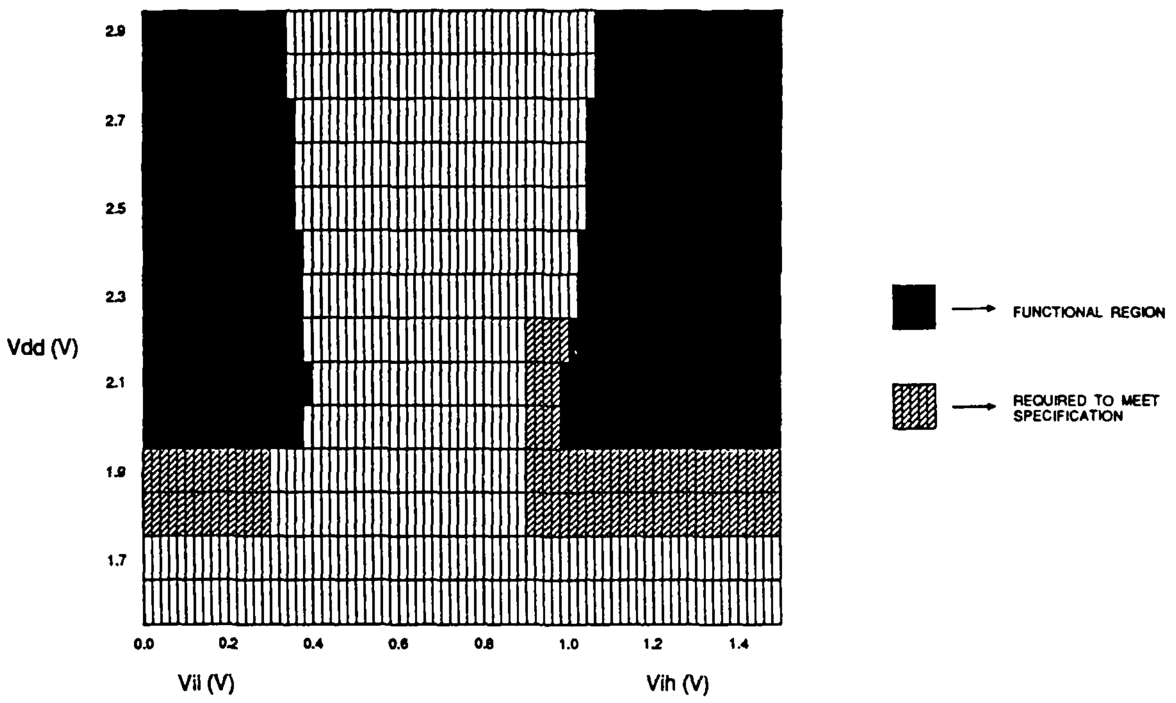
Table 10 — TRANSVERSAL FILTER CHIP PERFORMANCE

Device	min V_{DD}(V)	max V_{ol}(V)	min V_{oh}(V)	max V_{il}(V)	min V_{ih}(V)	I_{dd} (A)
(82, 2, 3)	1.9	0.035	1.330	0.365	0.981	2.45
(84, 5, 2)	2.0	0.069	1.297	0.463	0.928	3.06
(41, 7, 3)	2.2	0.042	1.285	0.325	1.136	2.60
DESIGN GOAL/SPEC	1.8	<0.2	>1.0	>0.3	<0.9	3.2

Because V_{ih} and minimum V_{DD} levels did not meet their design targets, we performed extensive analysis including the use of shmoo plots. This provided a better depiction of the devices' operating regions. Figure 8 shows an example of the type of plot generated for a functional device. No surprises or inconsistent operating regions were uncovered by the shmoo plots. A closer look was taken at the V_{ih} values and it was found that a large distribution of voltages was seen for the different inputs on a given die. Data analysis found no correlation with absolute position on the die or other design-related issues. At this point it is believed that the wide range of V_{ih} values is a result of process variation across a single die and possible testing anomalies.

In an effort to close the design/processing/test loop, analysis of the TFC wafers' PCM data was performed. Each tested die was assigned two values; one for the number of test vectors which passed and another for the number of bits which passed all test vectors. These two values were used as measures of functionality for the devices. Some correlation was seen between functionality and threshold voltage as well as functionality and EFET/DFET current ratio although the sample size is too small to reach any strong conclusions.

In summary, fully functional devices in excess of 41,000 transistors were found on both tested lots, proving that 5K gate circuits can successfully be fabricated in the AT&T Gallium Arsenide Pilot Line. This also marks a success for HCAD which now has been shown capable of designing into the DARPA Pilot Line. Finally, the previous Standard Cell Casino Test Chip (CTC) effort provided much knowledge and experience related to the design and test of high-complexity digital GaAs circuits. The lessons learned from the CTC contributed greatly to the success of the Transversal Filter Circuit.



Transversal Filter Chip Shmoo Plot of V_{il} and V_{ih} against V_{DD}

Figure 8.

3.9 Cell Array Casino Test Chip Design Using HCAD (S. W. White, L. R. Fisher, W. A. Oswald)

The Cell Array Casino Test Chip (CACTC) satisfies the contract's requirement for a deliverable gate array with 5.0K equivalent gate complexity. The design of the CACTC was a joint effort involving design teams at both AT&T and Hughes. AT&T's responsibilities included designing the cell array floorplan and library, while Hughes used HCAD to personalize the Casino Test Chip function onto the array. Both teams performed independent logic and layout verification to ensure an error-free design. Good communication between the two design teams enabled the successful completion of this task. This was accomplished through regular conference calls, face to face meetings, and electronic mail.

The CACTC is functionally equivalent to the Standard Cell Casino Test Chip previously developed by Hughes for the AT&T Pilot Line. As such, it contains the same functional circuitry including a Datapath, Switch Matrix, Programmable Multiplexer, Boundary Scan Register, and Ring Oscillator. Mentor formatted logic schematics from the older standard cell design were used as a baseline for the cell array implementation. These schematics were updated to reflect the cells available in the newly developed cell array library. This library contains most of the cells in the standard cell library but their implementations differ somewhat; the E-family of SFFL is used and dual-gate FET structures have been eliminated from all cell types.

In order to make optimal use of HCAD's capabilities, the updated Mentor CACTC schematics were translated into Cadence format rather than simply translating the netlist. Additional HCAD cell representations were created for logic, circuit, and fault simulation as well as timing analysis, layout, and verification. With a complete cell array library hosted within HCAD, the design was verified using the SILOS logic and fault simulator. The standard cell CTC's simulation vectors were used following a translation into the HCAD compatible STL format. Because AT&T required a netlist representation to perform logic and layout verification, an LSL netlister was written and is now a permanent feature of HCAD. The CACTC design was subsequently run through this tool to create a netlist compatible with AT&T's computer aided design environment.

Mentor's GateStation software, a key component of the HCAD system, was used to place and route the CACTC. Descriptions of the floorplan and cell layout personalizations were generated for GateStation in the form of text files. A number of test layouts were run but all resulted in many unrouted nets. After examination of these test cases, changes to the floorplan were recommended and later implemented at AT&T. GateStation is a row oriented, channel based router and thus works best with a floorplan of this style. The original floorplan was in a cell island style which explains why the router encountered such difficulty. The changes made to the floorplan reallocated the array's routing resource which greatly enhanced its compatibility with the router. Future routes on the enhanced floorplan were completed automatically with no unrouted nets.

Increased routing efficiency also was obtained by rotating the floorplan 90 degrees as represented within GateStation. This provided pin locations in the vertical plane that the router preferred. In the final GateStation session, the CACTC's I/O and Ring Oscillator cells were manually assigned to positions in the array by adding site locations in the schematics. All remaining cells were automatically placed and all nets automatically routed. Array utilization is quite high, exceeding 82%. The Hightower number is 55.

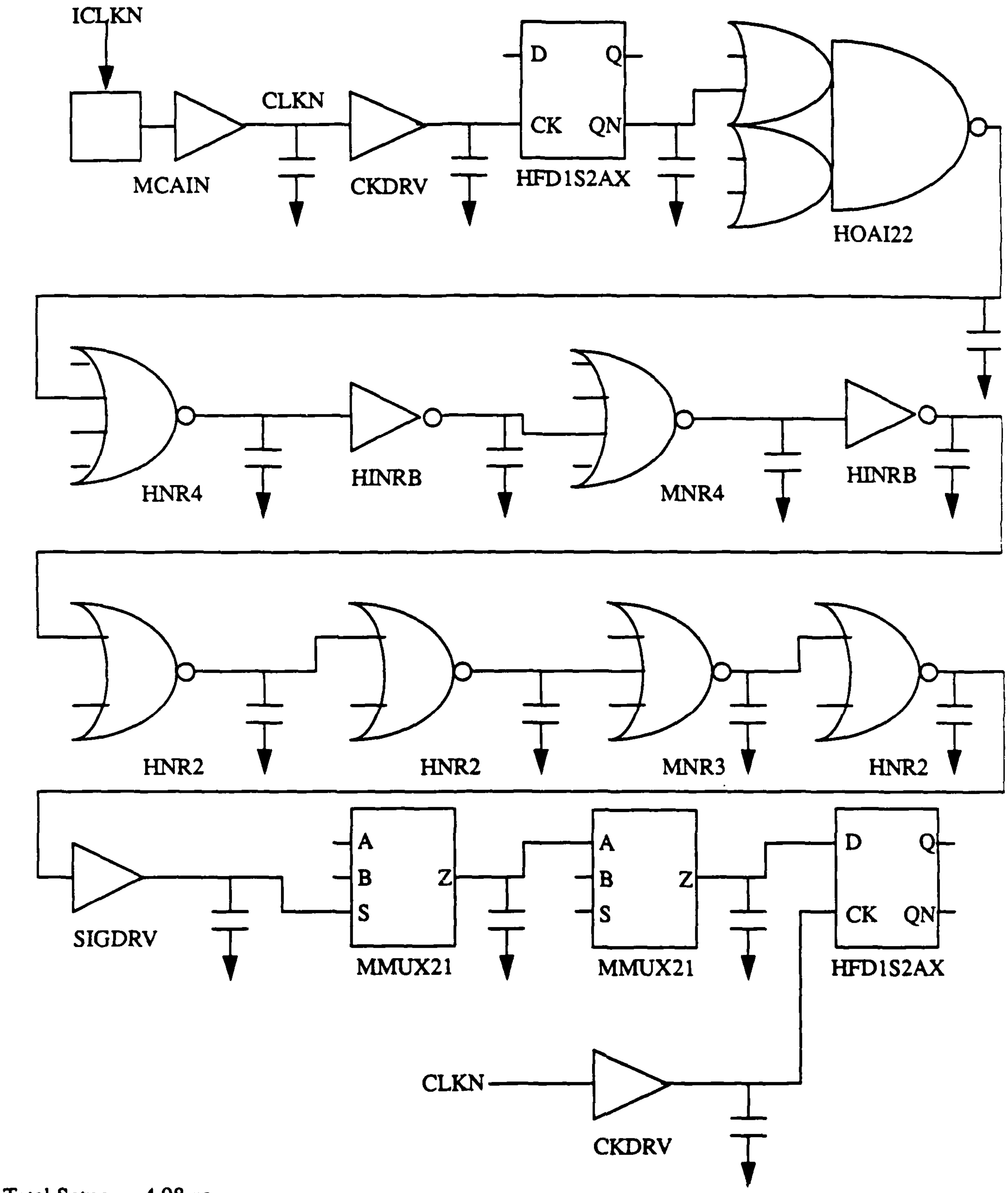
After HCAD successfully completed a fully auto-routed personalization, a timing analysis using the TA simulator was run to evaluate the effect of parasitics on the circuit's performance. TA identified the slowest paths within the design which prompted the addition of net weights into the schematic followed by a final iteration of the place and route process. Critical path nets were subsequently examined in the interactive routing environment and some were manually rerouted to minimize their lengths. Clock nets were given similar attention to eliminate the possibility of skew problems. By utilizing the net weights and HCAD's gate array interactive routing capability, the CACTC's critical path performance was improved by approximately 20%. The circuit's simulated performance is 199 MHz for a critical path that is 18 gates long. An ADVICE circuit simulation performed at AT&T predicted 204 MHz (272 ps/gate). Figure 9 is a diagram of the critical path.

Layout verification at Hughes consisted of design rule checking and two levels of layout vs. schematic checking (macrocell and device level). The final verified version of the CACTC layout was sent to AT&T for further independent verification using their own tools.

The final device size is 11,748µm by 11,744µm. During the final stages of design, we decided to cut the power bus between the input and output bonding pads. The Standard Cell Casino Test Chip (on which the 5K is based) was impossible to test due to power bus oscillation. The separated power bus will only help during wafer test. Once packaged, all V_{DD} and V_{SS} are tied together. Masks were subsequently ordered, and the initial CACTC lot entered the processing line in late March, 1990.

3.10 32-bit Multiplier Design (L. R. Tate, R. J. Niescier)

We completed layout of the 32-bit Floating Point Multiplier during this reporting period. A major challenge in the layout of this circuit was the development of a robust power distribution scheme. The power supply routing must be unobtrusive enough, so that its capacitance contribution is minimal, but large enough to adhere to the electromigration rules and to minimize ohmic drop to the center of the chip. Two large horizontal topmet V_{DD} and V_{SS} busses are at the top and bottom of the chip to reduce ohmic losses and distribute power from the pads easily. Thirty two columns of 50µm V_{SS} and 20µm V_{DD} run vertically to supply the individual cells of the chip. V_{SS} is much wider that V_{DD} because the logic family can withstand a larger ohmic drop from the V_{DD} line than the V_{SS} line. The V_{DD} line is electromigration limited and the V_{SS} line is ohmic drop limited.


ICLKN
CLKN
MCAIN
CKDRV
D
Q
CK
QN
HFD1S2AX
HOAI22
HNR4
HINRB
MNR4
HINRB
HNR2
HNR2
MNR3
HNR2
SIGDRV
A
B
S
Z
MMUX21
A
B
S
Z
MMUX21
D
Q
CK
QN
HFD1S2AX
CLKN
CKDRV

Total Setup = 4.98 *ns*
= 271.7 ps/gate (18 gates in critical path)

Critical Path of Cell Array Casino Test Chip

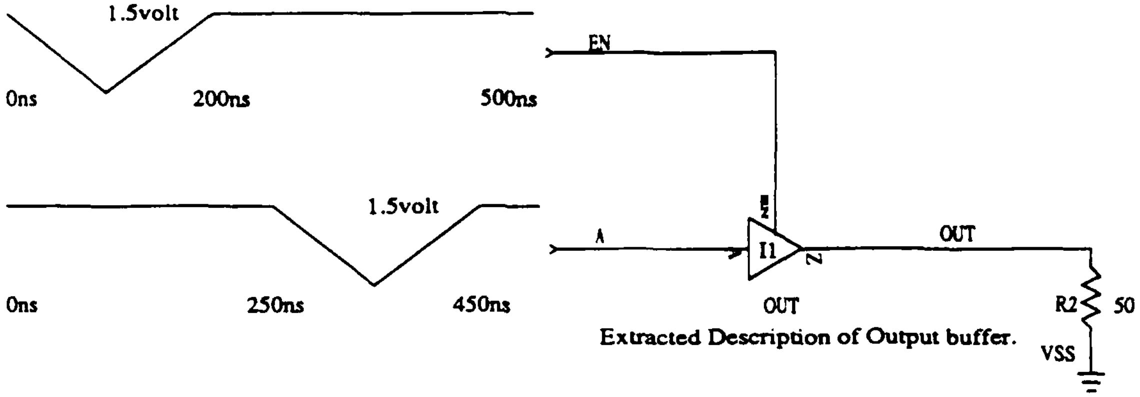
Figure 9.

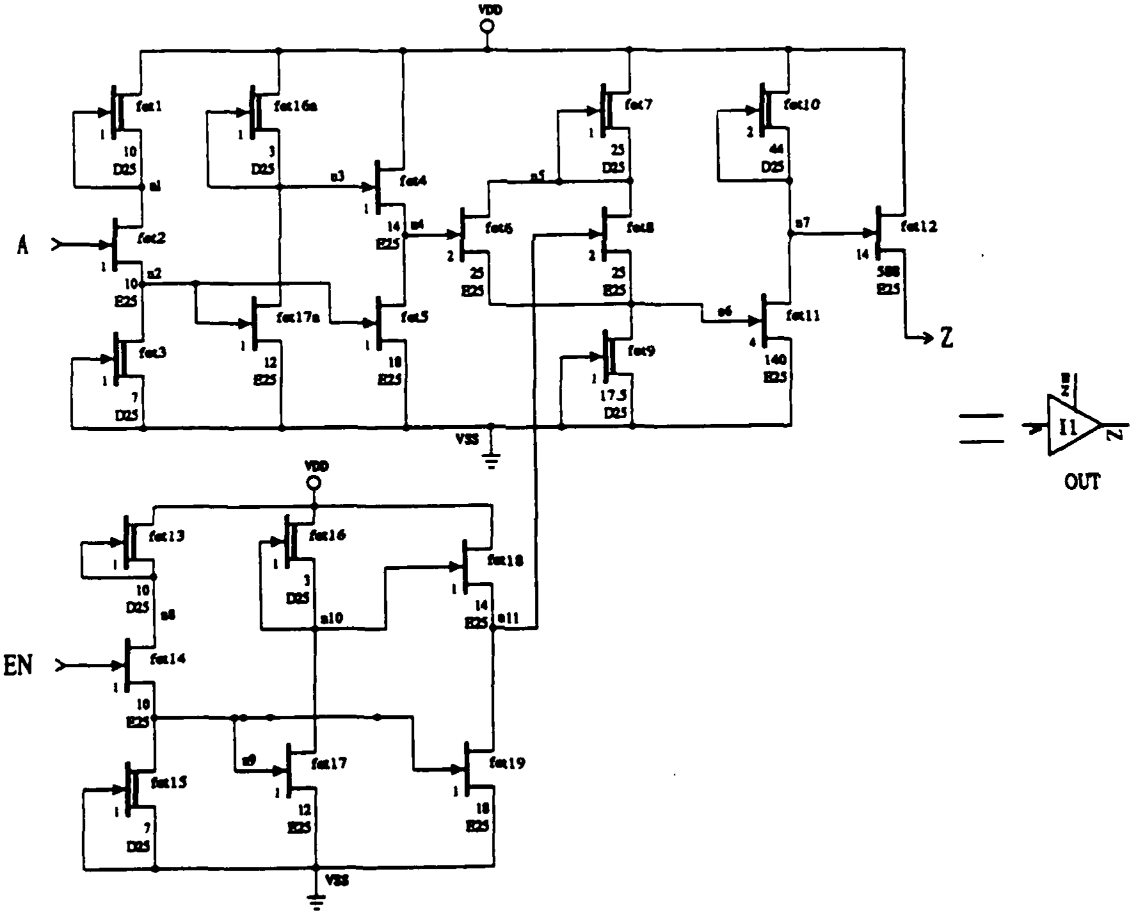
An electromigration and ohmic loss analysis was performed on the worst case column in the chip. The results show worst case losses of 36 mV on the ground buss and 90 mV on the V_{DD} Bus. The ohmic loss analysis assumed an isolated worst case column with a worst case current flow and 0.04 ohms/square for topmet. A sub-power network of six micron botmet lines is not included in the analysis, so the resultant losses are expected to be slightly better than predicted.

A first order calculation of the power dissipation showed a worst case power dissipation of 8 watts with the I/O drawing about 3 watts. This analysis assumes that every column needs the same amount of current as the worst case column and all I/O draw their maximum current. This GaAs chip design contains four slightly different source-follower logic families, optimized to perform specific purposes within the design and help trade off speed, power, and density. Every gate's design on this chip was separately extracted and simulated with nine different capacitance and fanout loading conditions under all six ADVICE model parameters which include 25 and 125°C models. This resulted in over 1600 gate simulations with each input of every gate being fully exercised. These simulations were necessary to assure that every gate would perform properly over all expected conditions (including temperature), and interface properly with the other logic families in the design.

The critical path consists of 78 separate gates and occurs under only a few special conditions. The worst case delay occurs when the exponent overflows due to the incrementer rounding into the 47th bit, changing it from a zero to a one. Like the gates, the critical path of the multiplier was extracted with capacitance from the layout and simulated over all model files. Because of the number of transistors and capacitors in the fully extracted critical path, the ADVICE file was too large for ADVICE to handle (over 7000 transistors). We broke the simulation into three smaller parts. The results of the simulation predict a worst case delay of about 13.5 nS, with a best or typical case being about 8.5 nS (109-173 ps/gate).

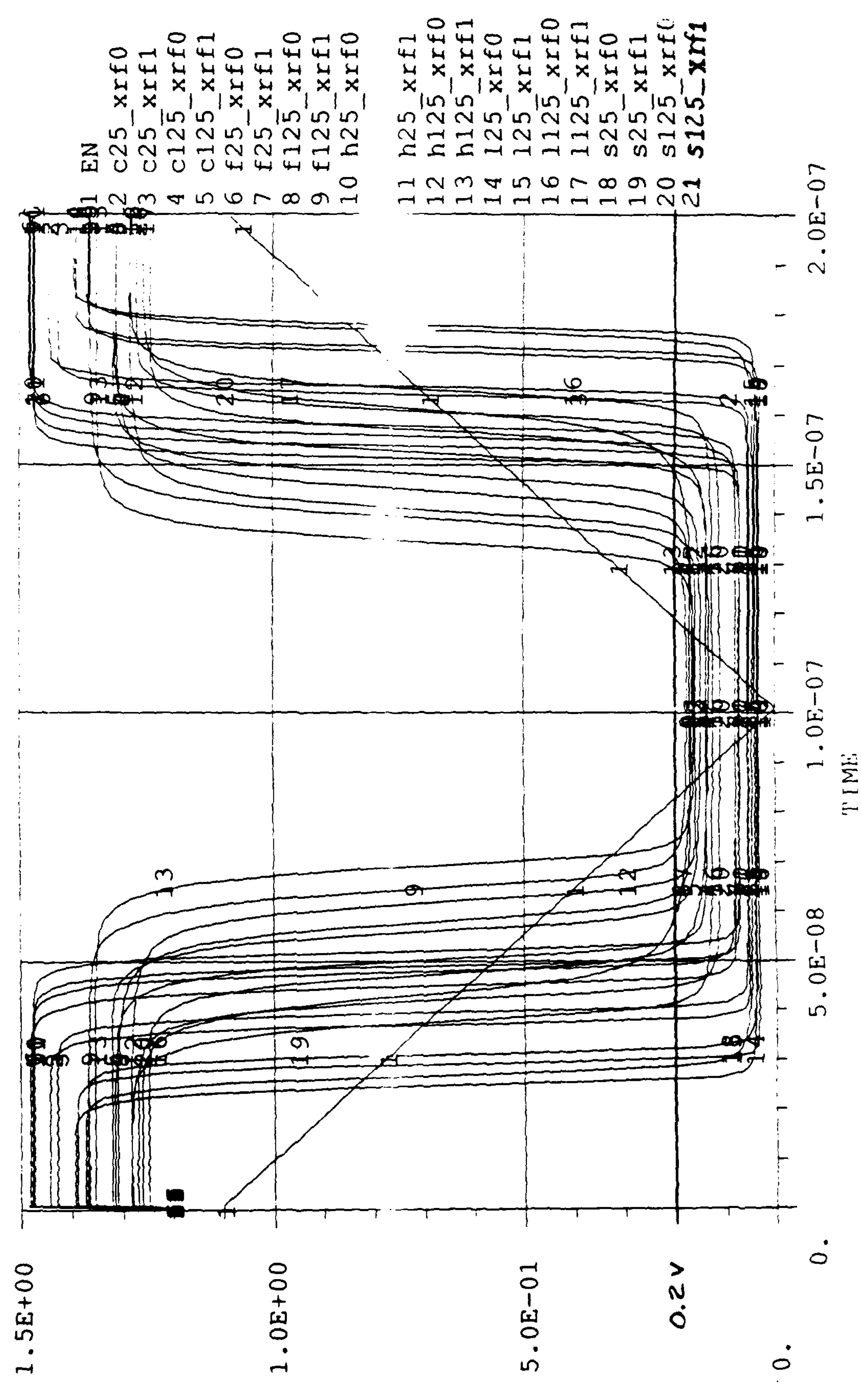
Output buffers were designed to satisfy the DARPA specifications over all simulation files. The primary design objectives were to provide solid logic low ($V_{ol} < 0.2V$) and logic high ($V_{oh} > 1.0V$) levels over temperature while keeping power consumption to a minimum. Power consumption was minimized by using small devices in the initial stages of the buffer. This results in slower switching speed and some slight (0.03V) degradation of worst case logic high levels. Simulation showed that a driven DFET stage just prior to the main output transistor did not improve the logic levels and increased power consumption as compared to a DCFL stage - hence we chose the latter. The Schematic of Figure 10 shows the setup for a slow ramp ADVICE simulation. Figure 11 shows that for all combinations of high and low threshold voltages and for all combinations of frequency dependent output conductance the logic lows are less than 0.2 volts. The worst case (#9) is low thresholds for both EFET and DFET at 125C. The Logic highs are all above 1.2 volts. The switch points range from 0.4V to 0.9V and are centered at about 0.65V.


1.5volt
0ns
200ns
500ns
EN
1.5volt
0ns
250ns
450ns
A
EN
I1
Z
OUT
OUT
R2
50
VSS
Extracted Description of Output buffer.


VDD
fet1
fet16a
fet4
fet7
fet10
fet12
A
fet2
fet6
fet8
fet3
fet17a
fet5
fet9
fet11
n1
n2
n3
n4
n5
n6
n7
Z
VSS
I1
EN
Z
OUT
VDD
fet13
fet16
fet18
EN
fet14
n8
n10
n11
fet15
fet17
fet19
n9
VSS

32-bit Floating Point Multiplier Output Buffer Slow Ramp Simulation

Figure 10.



Simulation of Output Buffer for 32-bit Floating Point Multiplier

Figure 11.

4. PILOT PRODUCTION

4.1 MBE Process Status and Modified Process (H. H. Vuong, C. L. Reynolds)

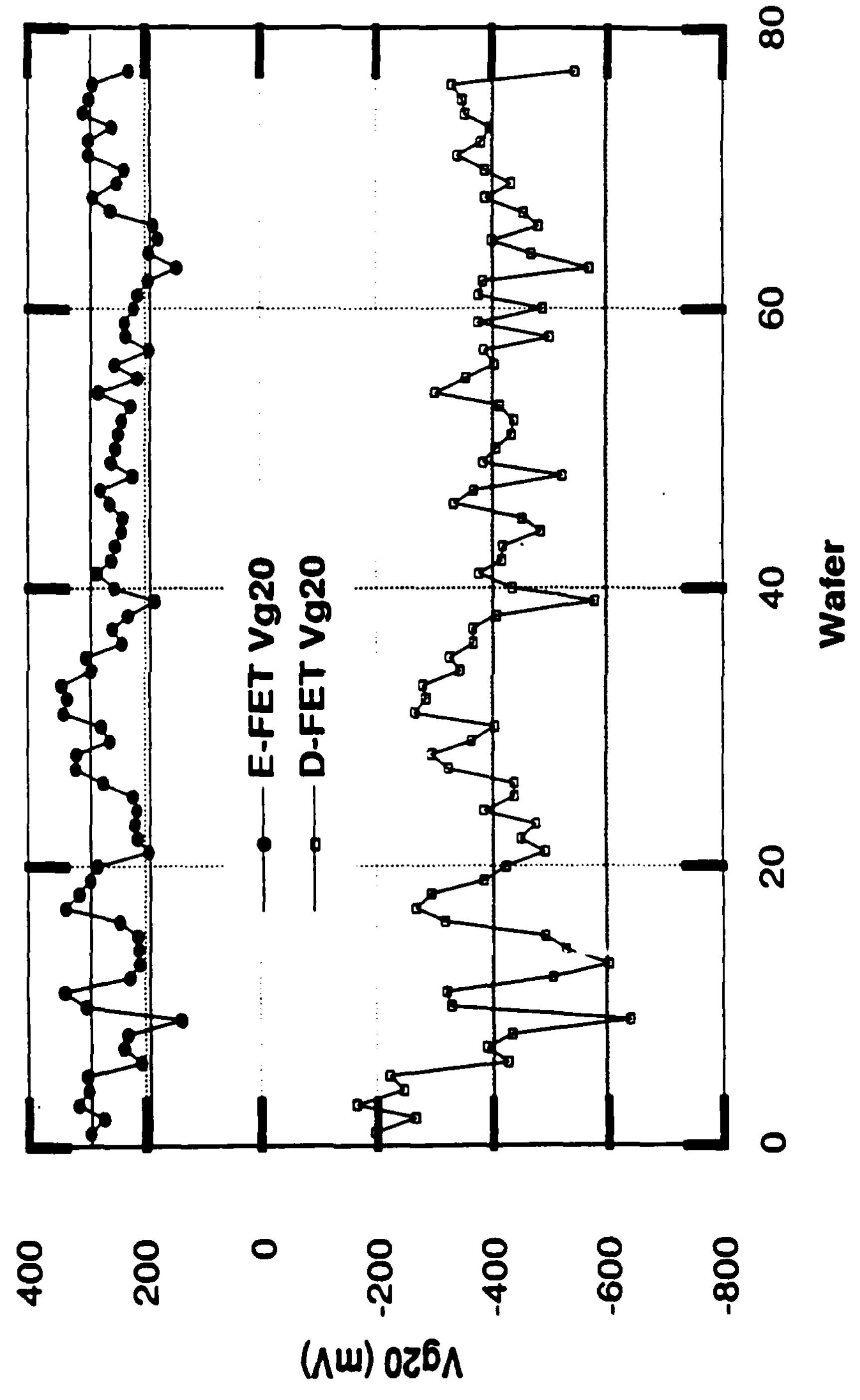
Since October, 1989, 241 wafers were shipped to the processing line for the Pilot Line III program. As mentioned in the last report, the layer thicknesses were adjusted to center the threshold better within the target window. Both EFET and DFET parameters show improved agreement with the target windows. In particular, the EFET threshold voltages are well centered, while those for the DFET are 50-100 mV too positive (see Figure 12, where the solid horizontal lines indicate the design targets). The discrepancy for the DFET is related to failure of the MBE model as discussed in Section 4.3 of this report.

During the first portion of this reporting period, throughput from the MBE area was hindered due to a plant power failure. As a result of the power glitch, the sources cooled rapidly from idle temperature, and the group III crucibles cracked. This situation necessitates bringing the growth chamber to atmospheric pressure and reloading sources. During this reporting period, we also identified shutter alignment as critical for intra-wafer uniformity.

Growth efforts have now converged to provide a revised structure, ED11, which incorporates the ozone clean of the substrate and yields the target threshold voltages and channel currents with minimal sidegating. Impact of Si at the interface has been reduced by use of a pre-buffer. These adjustments to the structure have been implemented under change control, and results to date look promising. A complete analysis will be done after an adequate number of wafers have been fully processed.

4.2 Pilot Line Throughput, Interval, and Yield (J. H. Duchynski, S. M. Parker)

During the last six months, 233 wafers were started in Pilot Line III. One hundred sixty-five wafers were completed through processing and were PCM tested in that same time period. Starts were made in the baseline SARGIC technology for the following codes: PT-1, PT-2M, Custom ALU, 1K Cell Array, Standard Cell ALU, Transversal Filter Chip (TFC), 4K SRAM, and Cell Array Casino Test Chip. No starts were made in the SARGIC Advanced Technology (APT-1 and APT-2). Wafer completions, however, occurred for both the Baseline and the Advanced Technologies. Table 11 summarizes the starts and completions by code for this reporting period.



Wafer Average Threshold Voltages for ED10 MBE Structure

Figure 12.

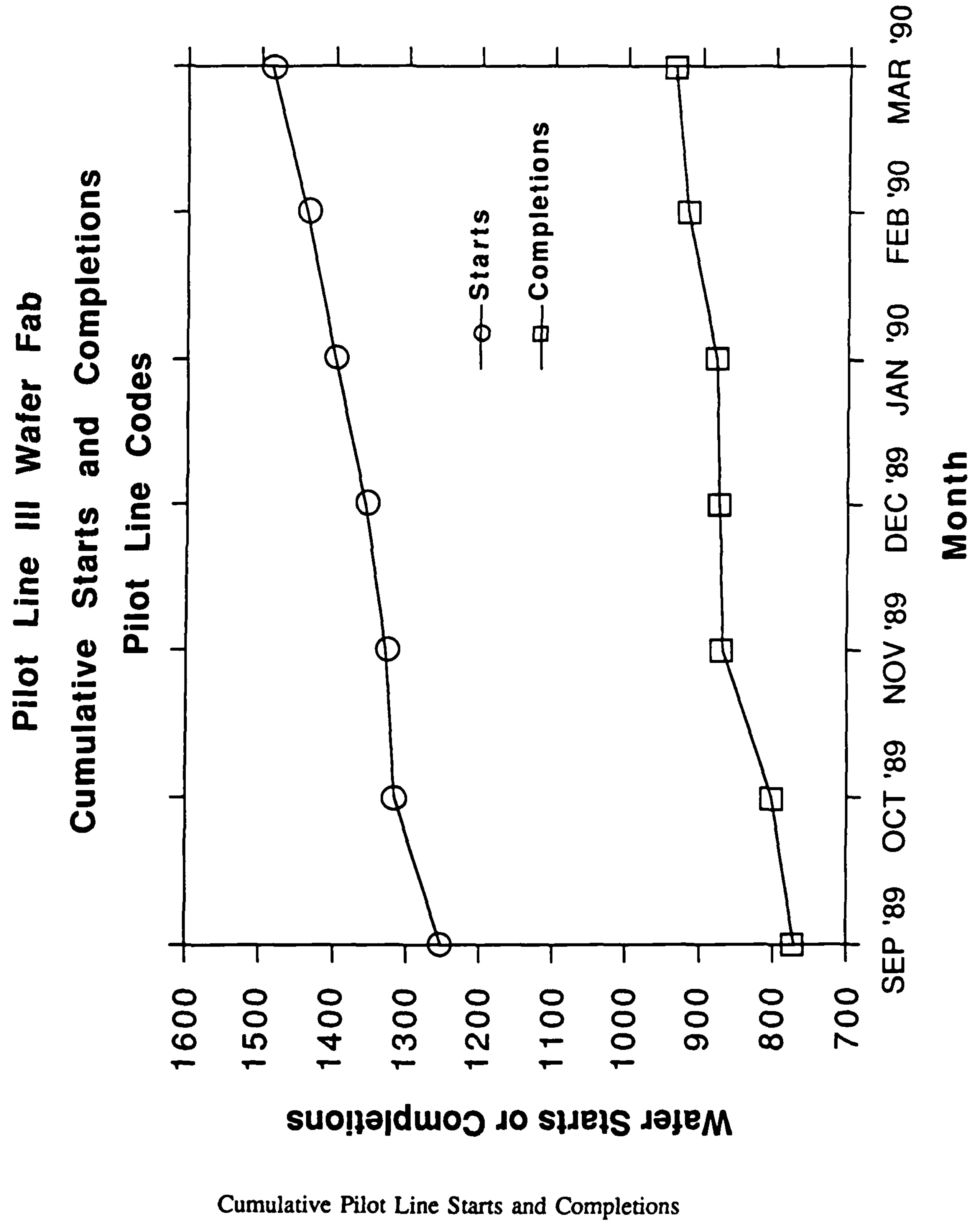
Table 11 — PILOT LINE ACTIVITY

Code Name	Wafers Started	Wafers Completed
PT-1	15	0
PT-2M	38	28
Custom ALU	42	39
1K Cell Array	6	11
Standard Cell ALU	30	23
TFC	36	24
4K SRAM	60	17
5K Cell Array	6	0
APT-1	0	11
APT-2	0	12
	233	165

The cumulative Pilot Line wafer starts and completions up through fiscal March, 1990, are shown in Figure 13. Thus far, 1486 wafers have been started and 937 wafers have reached completion. Additional wafers were started on the Pilot Line for other AT&T projects which involved SARGIC as well as other technologies. As of the end of March, 1990, total cumulative starts across all technologies were slightly above 2,900 wafers, and more than 1,500 wafers have been completed through PCM testing. Wafer starts combined for all projects increased on average from 20 wafers/week for the last reporting period to 33 wafers/week for this reporting period. The number of starts was higher due to less MBE machine downtime during the last six months as compared to the preceding six months.

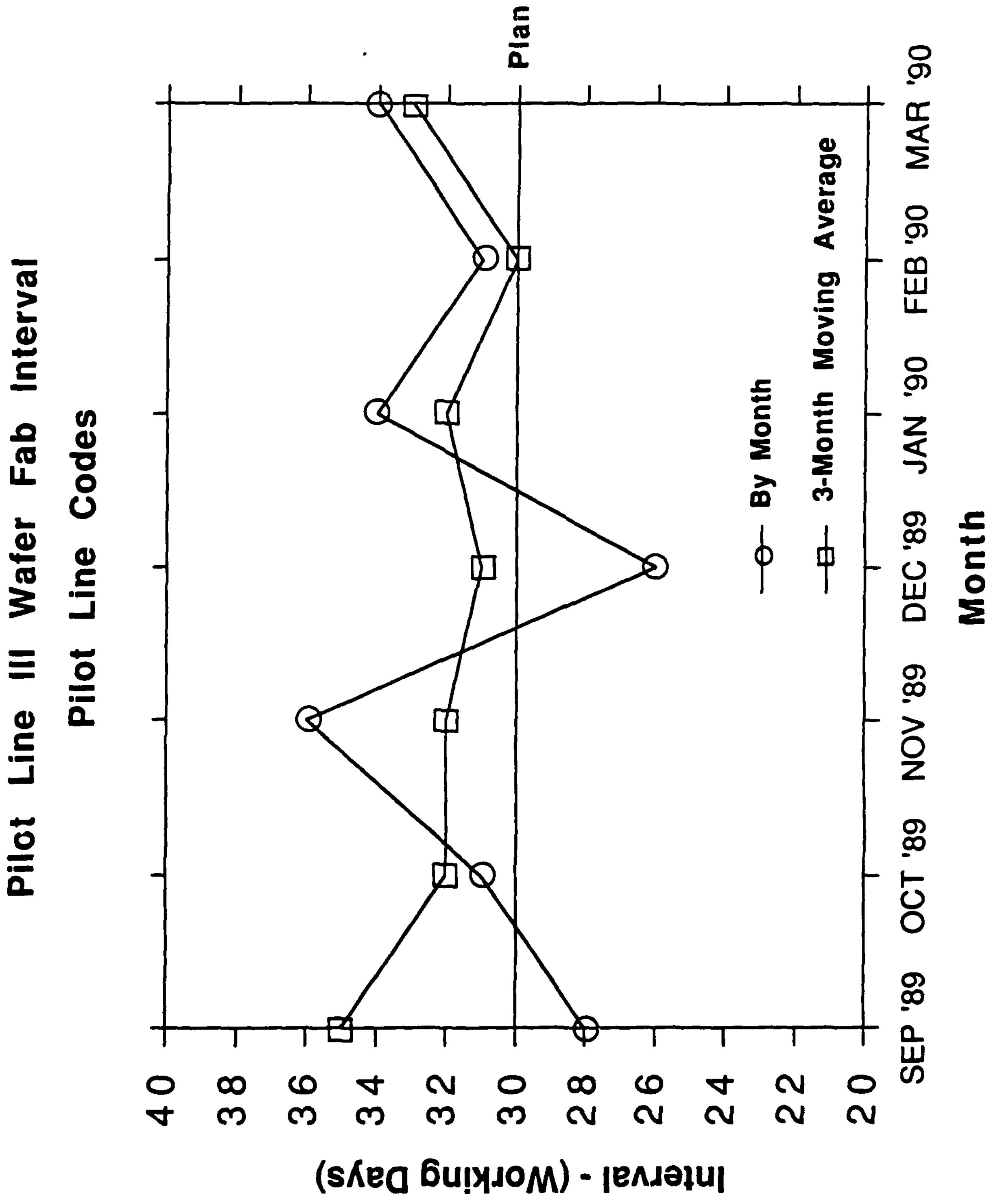
The fabrication interval for the Pilot Line codes is shown in Figure 14. The average interval for March, 1990, was 34 working days. This is an increase compared to the 28 day interval accomplished during September, 1989 period. The interval climbed to 36 days in November due to photoresist developing problems at the gate level which caused a substantial amount of photoresist rework to be performed. During late November and early December, the MBE system was down for a source reload which resulted in fewer wafers entering the line. Consequently, the December interval dropped down to an artificially low value of 26 days. Once again, the interval rose to 34 days in January and in March due to SiON etch equipment downtime and SiON deposition equipment downtime, respectively.

Figure 15 shows the wafer throughput or fabrication yield for the Pilot Line codes. This yield is actually a mechanical yield which compares the number of wafers successfully reaching PCM testing to the number of wafers originally starting in the fab line. For most of the reporting period, the yield fluctuated around 90%. Lower yields were experienced in November and December due to wafer warpage which occurred in the high temperature anneal furnace. The average yield for every month in



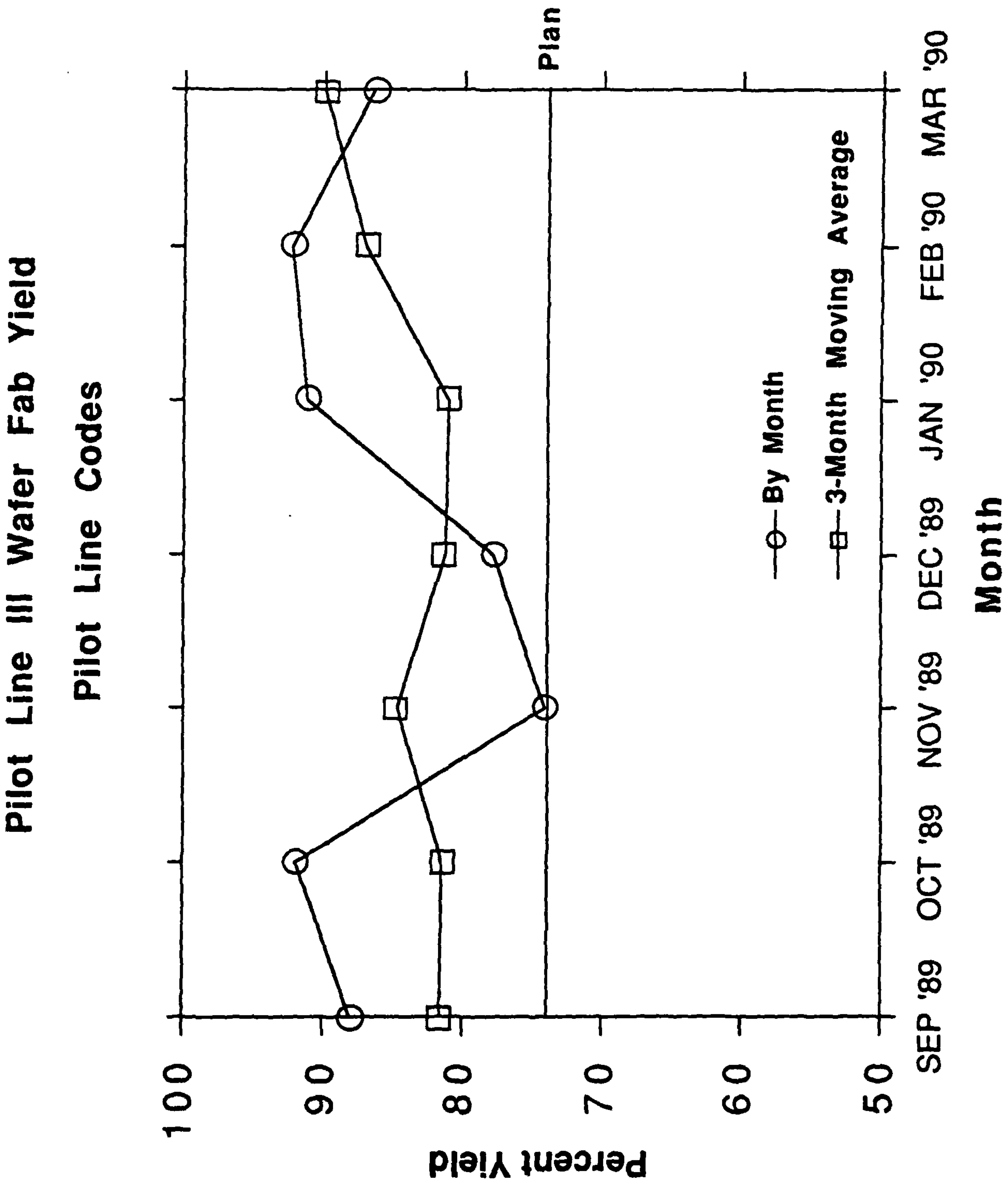
Cumulative Pilot Line Starts and Completions

Figure 13.



Pilot Line Wafer Fabrication Interval

Figure 14.



Pilot Line Fabrication (Mechanical) Yield

Figure 15.

the reporting period, however, remained above the target plan yield of 74%.

4.3 Baseline Technology, Threshold Control, Processing Issues (C. L. Reynolds, H. H. Vuong)

After the major improvements which were implemented in 1989, the variation of FET parameters continued to be small. As mentioned in Section 4.1 of this report, the EFET threshold voltage for ED10 is well centered within the target window while that for the DFET is too positive. Figure 16 shows the difference between the measured and predicted threshold voltages. The distribution for the EFET is centered near zero, which is optimum, and that for the DFET is centered around ~60 mV. This discrepancy is significant with respect to the target window and is consistent with a shift calculated for the effect of a carbon impurity layer at the interface. Some positive shifts of threshold voltage with the ED10 structure have been correlated with eddy current sheet resistances (R_s) which are too large, and thus, a specification on R_s after MBE growth has been initiated.

Preliminary analysis of the ED11 structure has been completed, and significant differences were observed for several important parameters. The ED11 structure is closer to target than ED10 for the DFET threshold voltage and current, the EFET and DFET breakdown voltages, and the EFET and DFET sidegating currents. The ED11 EFET threshold and current are about the same as ED10 (that is, they are on target). The ED11 structure also shows softer pinchoff characteristics than ED10.

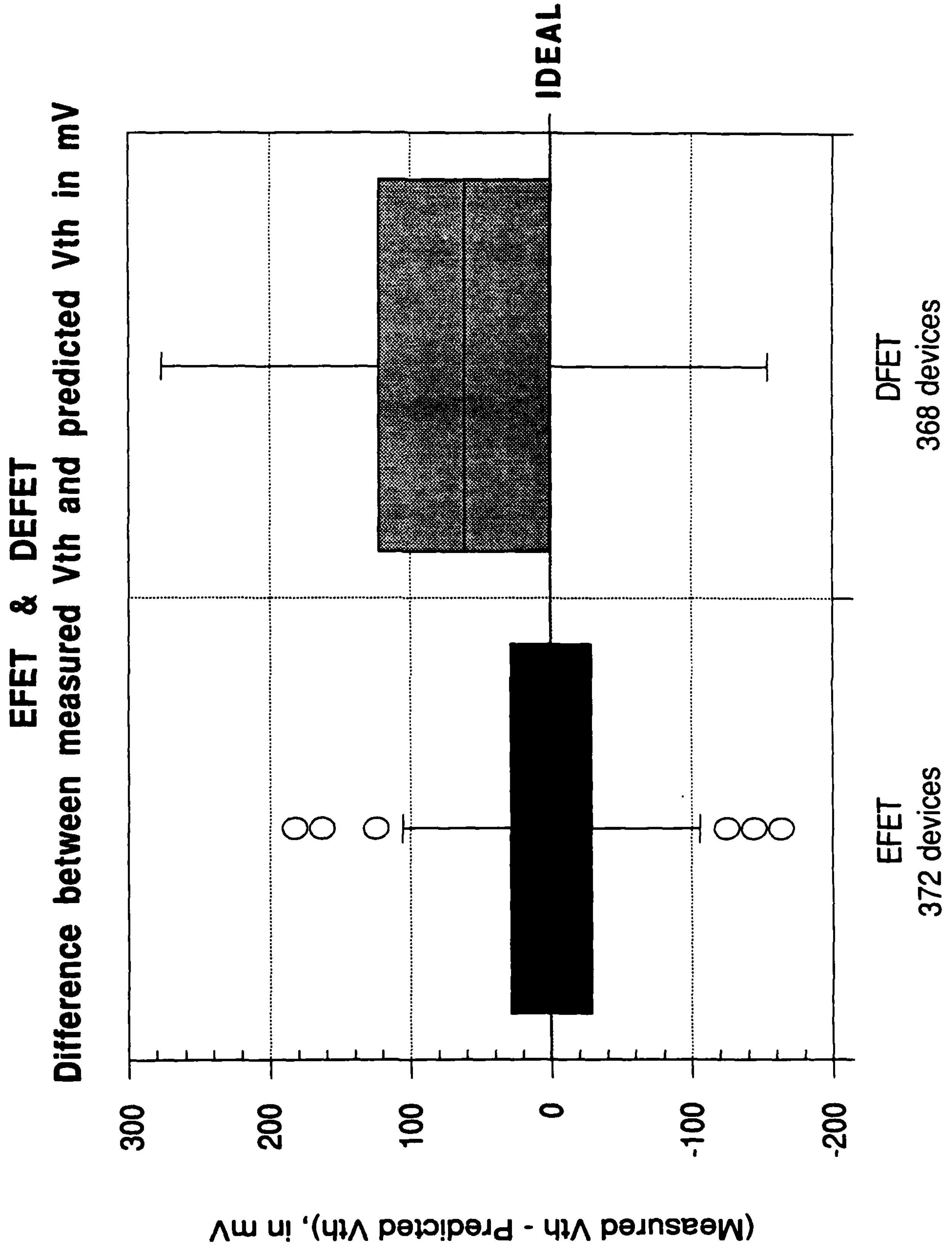
Several key issues with respect to the DARPA baseline technology arose during this reporting period. A re-entrant via profile was found to cause poor step coverage of the interconnect metal. The via profile had changed as a result of contamination in the etch chamber, which has now been cleaned. Optimum etch conditions were then determined by means of a statistically designed experiment, and the via contact resistances have returned to their normal, low values. The via profile problem resulted in several flawed wafer processing lots, thereby delaying analyses of primary circuit characteristics.

New process controls have been or are being implemented for the furnace, ohmic metal, and pre-gate processes. Validity of the FET test data has been questioned, and tests have been initiated to ensure proper probe pressure.

As device width is varied from 50 to 3µm at constant gate length, DFETs show good scaling behavior while EFETs show degradation. Experiments have shown that EFET scaling is improved when no EFET tubs are fabricated. As the scaling problem affects all present circuits, a solution is needed. The problem is under active investigation.

4.4 PCM and Circuit Yield (C. H. Tzinis, W. R. Ortner)

Data analysis of PT-1 memory and especially PT-2M proved instrumental in model validation and in establishing correlation between PCM parameter and circuit test



Comparison of Measured and Predicted Threshold Voltages for ED10 MBE Structure

Figure 16.

yields. Figure 17 demonstrates that for high circuit yield, the FET characteristics (EFET and DFET thresholds and currents) should be in a threshold window close to the one predicted by the model. In addition, empirical analysis shows that maximum yield occurs when the threshold and corresponding current follow a linear relationship (approximately constant gm) both for EFET and DFETs. Based on this analysis, criteria were established for screening wafers prior to circuit testing; these criteria are summarized in Table 12.

Table 12 — PCM CRITERIA

Parameter	Range	Units
EFET I_{ds}	$40 \le I_{ds}^{E} \le 70$	mA/mm
DFET I_{ds}	$70 \le I_{ds}^{D} \le 120$	mA/mm
Via Resistance	$4 \le R_{via} \le 20$	kΩ/4000 vias

Using these criteria, the fractional yield on a per code basis and total is shown in Figure 18 for the last six months. The low yield observed in the last quarter is due to the via problem described in Section 4.3.

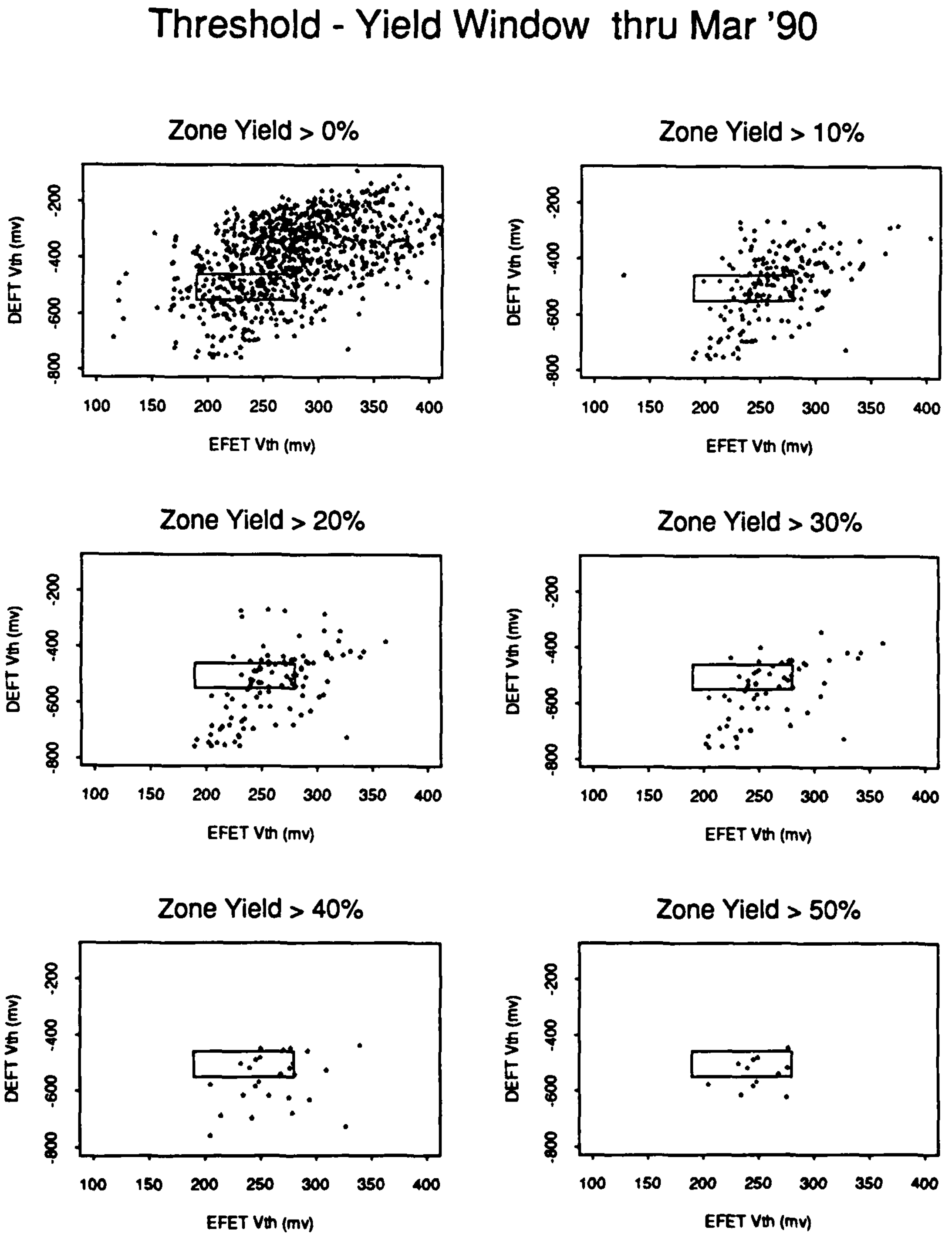
Figure 19 shows the average PT-2M circuit yield per wafer as a function of the number of good PCM sites for a wafer; the number on top of the bar denotes the sample size for the distribution. There is a strong tendency for good PT-2M circuit yields to come from wafers with high PCM yields. On the other hand, we do not see such a correlation for logic circuits (Custom ALU, Standard Cell ALU, TFC, 1K Cell Array). We are presently working to develop a PCM test suitable for predicting logic circuit yield.

4.5 Advanced Technology (A. G. Baca, R. J. Shul, A. L. Helms, R. J. Niescier, S. F. Nygren)

The Advanced Technology differs from the Baseline Technology in three important ways: It uses aluminum interconnect metallization, interconnect metallization design rules are decreased to 1.5 µm lines and spaces, and logic design uses an improved implementation of the SFFL logic gate. Except for reliability studies, we completed our investigation of the manufacturing feasibility of this Advanced Technology. This section reports the development and characterization of wafer processing procedures, and a description of circuit test results. Radiation hardness results are reported in Section 5.1.

Process Development

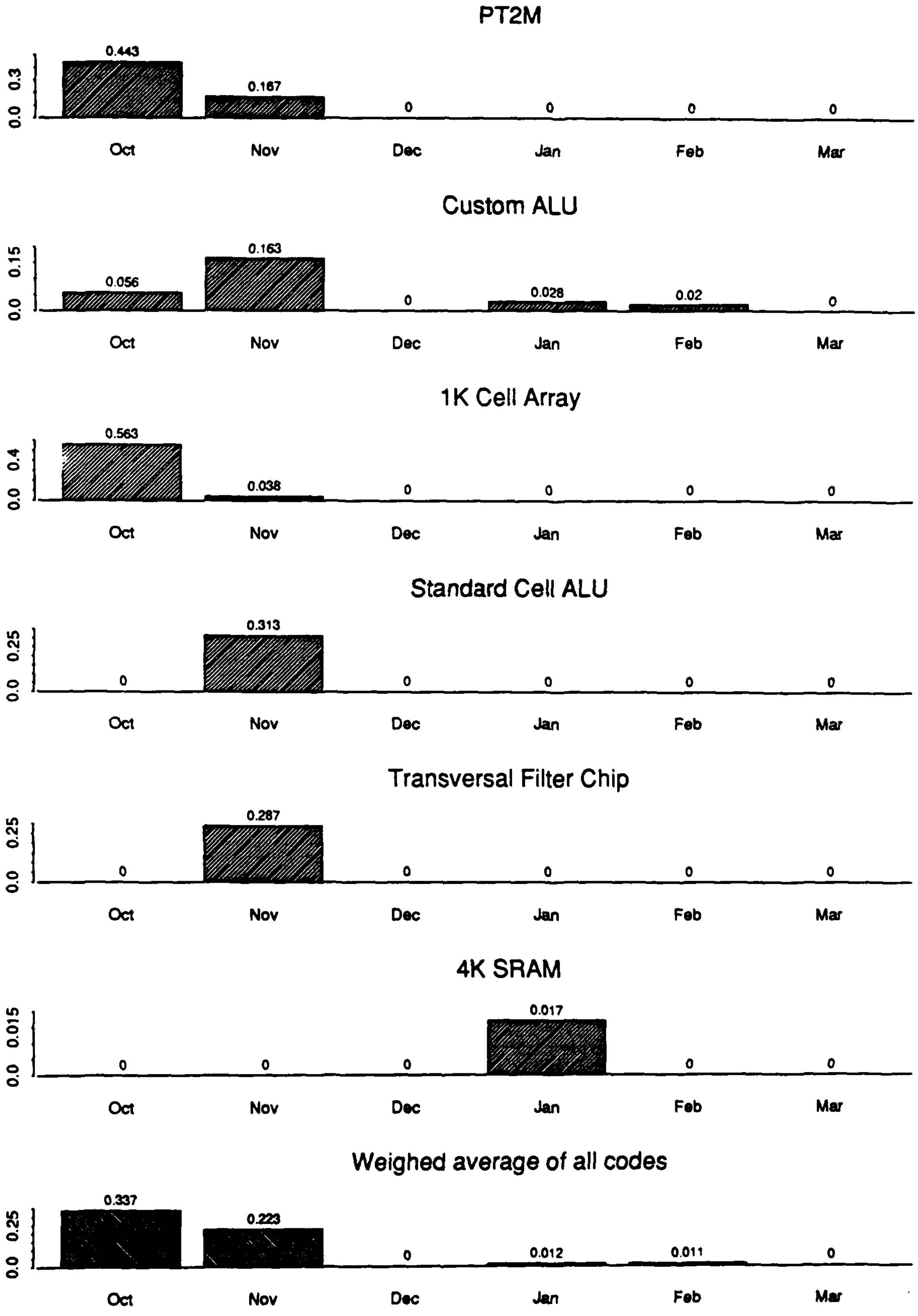
In the previous report, we described processes for sputter depositing aluminum metallization, patterning it into 1.5 µm lines and spaces, using WSi as a barrier between the gold-based ohmic contacts and the aluminum interconnects, and applying



Boxed Area is sargic.11 Model Vth's Used to Design PT-2M

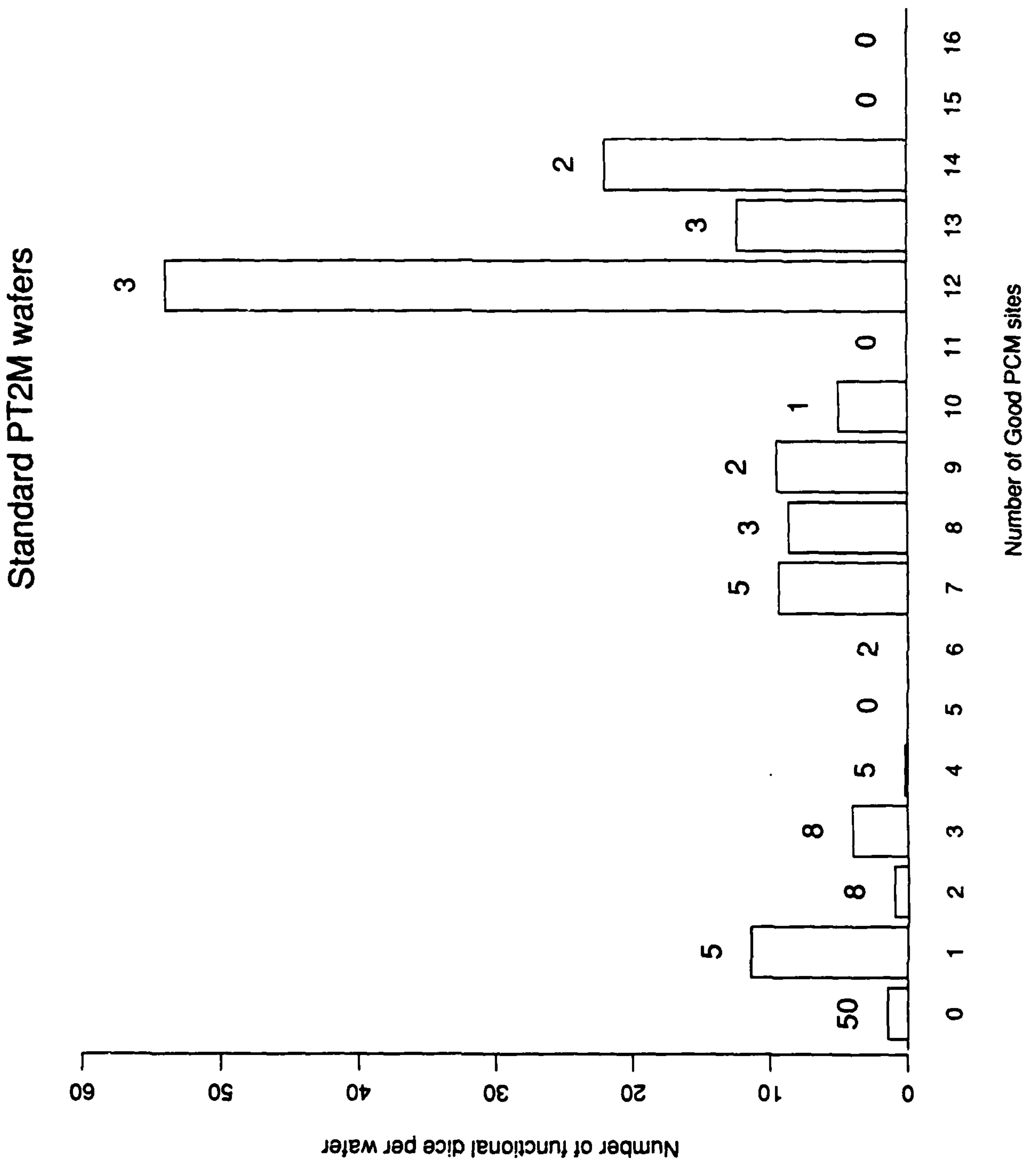
Process Window Defined by PT-2M Yield

Figure 17.



PCM Yields for October, 1989, through March, 1990

Figure 18.



PT-2M Memory Yield Compared to PCM Yield

Figure 19.

sidewalls to gate metal to eliminate aluminum stringers during the definition of bottom metal. We have now extended the process to include sidewalls on bottom metal to prevent stringers during the definition of topmetal.

We found that we needed to add planarization to the above sequence. Without planarization, there is about a 1:1 width-to-depth aspect ratio to the trough between metal runners with sidewalls after second dielectric is deposited. When topmetal is patterned, the aluminum is not consistently removed from this trough. To alleviate this problem, we developed a fully planarized interlevel dielectric. Following gate and ohmic metallization, we deposit a 10,000 Å layer of SiON. The SiON conforms to the contours of the metals, leaving a non-planar surface. We then spin-on 10,250Å of photoresist, leaving a planar surface. Finally, we use a CF_4/O_2 etch to thin the photoresist and SiON at virtually identical rates. This leaves 4000 Å thick, planar SiON over the gate and ohmic metal (see Figure 20).

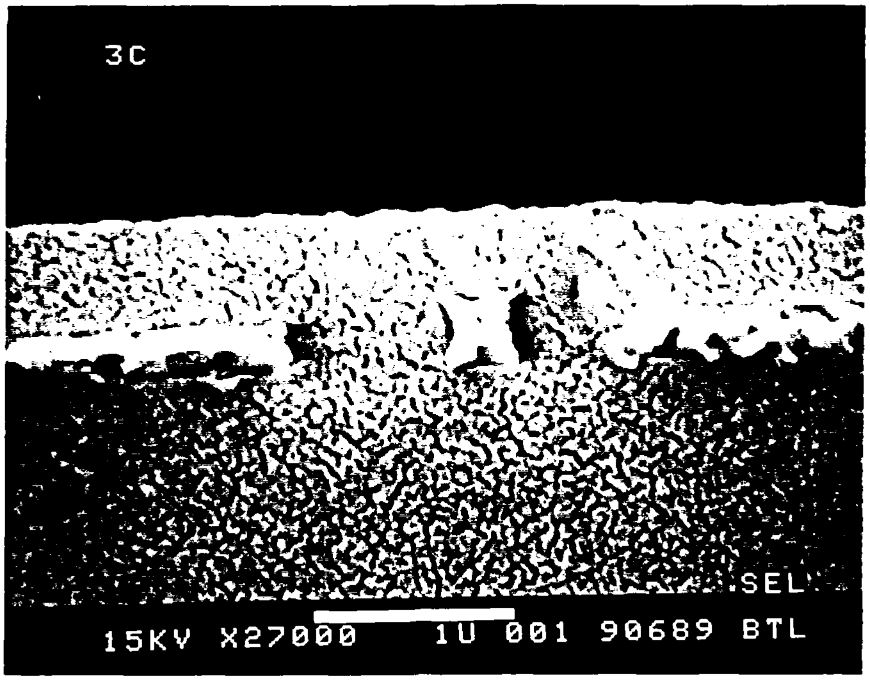
This completes development of the processes needed for the Advanced Technology. If this process were to be placed into production, two further steps would be needed: First, the interlevel dielectric planarization process must be integrated with the rest of the process. Second, we have seen burrs in the liftoff of the thin WSi used as a barrier between gold and aluminum. We need to develop a plug process that will function as a barrier to diffusion and purple plague, eliminate liftoff of sputtered metal, and improve the topography. As it is, only investigation of manufacturing feasibility is needed, and this is complete. Test results are given below.

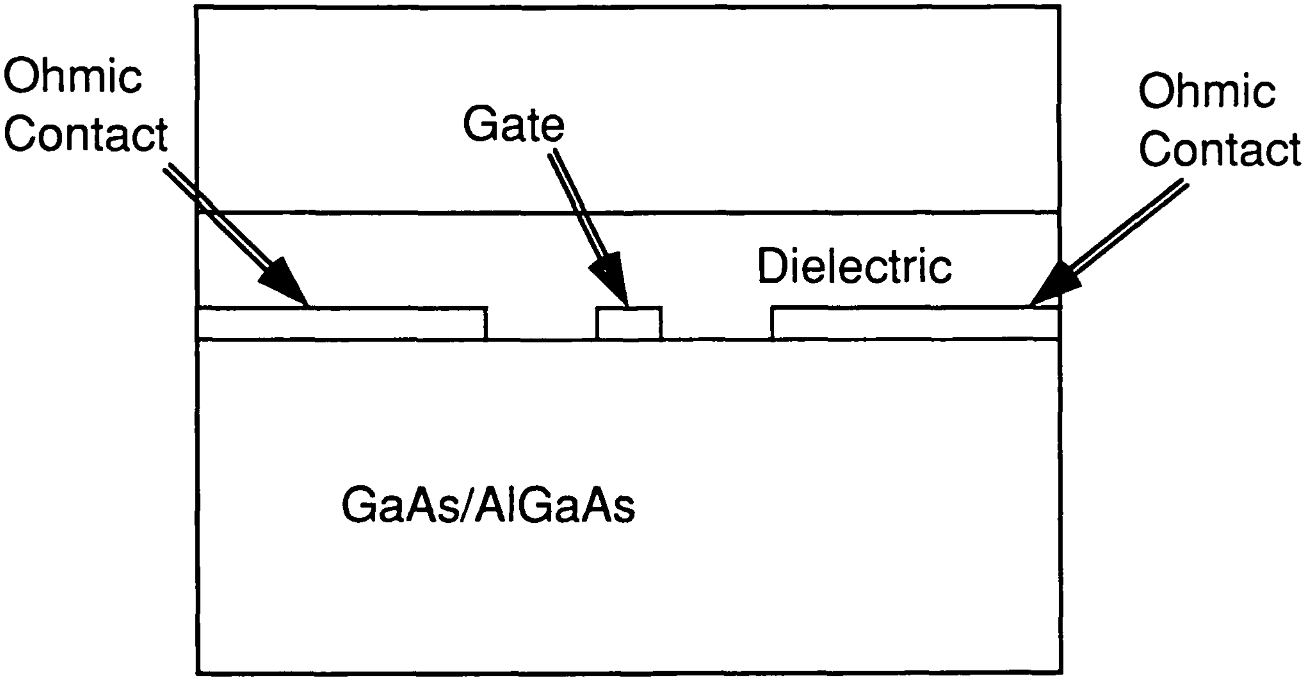
Process Characterization

One variation of the Advanced Technology uses 0.75 µm gate lengths. Figures 21 and 22 show inter- and intra-wafer variation of threshold voltages for EFETs and DFETs from 21 wafers in 5 lots. The variation is 2-to-3 times greater than for the Baseline Technology. As in the Baseline Technology, we expect we could reduce this variation through process analysis and process improvement. However, short channel effects are responsible for the major part of this variation, and a process enhancement like a lightly-doped drain structure will be required to further reduce the variation.

We characterize the Advanced Technology metallization with a new process tester called PT-Y. Metal shorts within a process level are tested by serpentines interleaved with combs using up to 19 cm of adjacent metal. A good serpentine/comb is one that has no shorts. Dielectric integrity and shorts between metal levels are tested by combs and serpentines on different levels with up to 250,000 crossovers in 1.5 µm design rules and up to 181,500 crossovers in 2.0 µm design rules. Again, a good tester is one that has no shorts. Finally, vias are tested by serpentines connecting different metal levels with up to 250,000 vias in 1.5 µm design rules and up to 181,500 vias in 2.0 µm design rules. A good via tester is continuous and has the proper resistance. All data are normalized to 250,000 vias or crossovers.

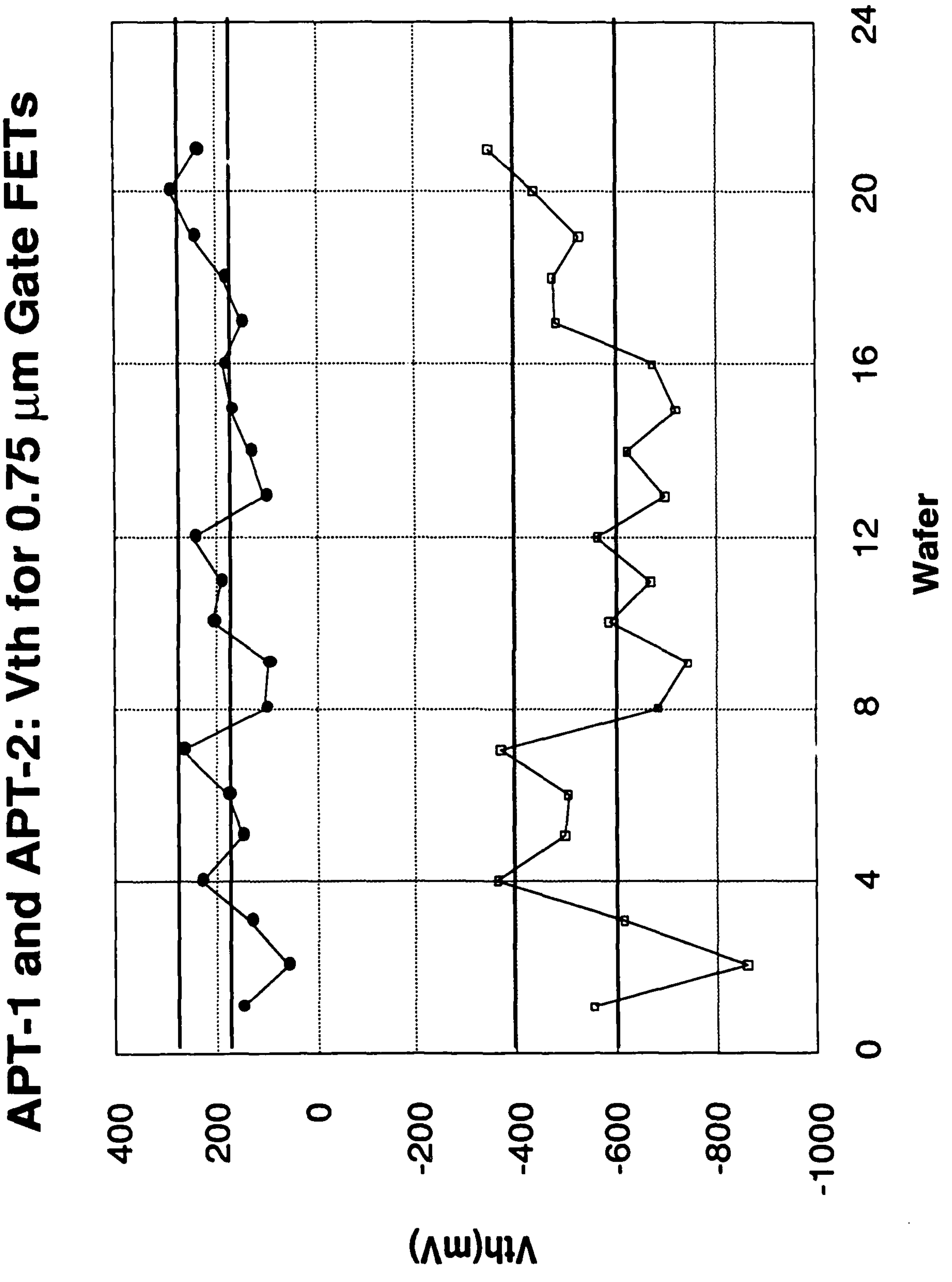
For 1989, data for gold interconnects are taken from 20 wafers processed in 4 PT-Y


3C
SEL
15KV X27000 1U 001 90689 BTL


Ohmic Contact
Gate
Ohmic Contact
Dielectric
GaAs/AlGaAs

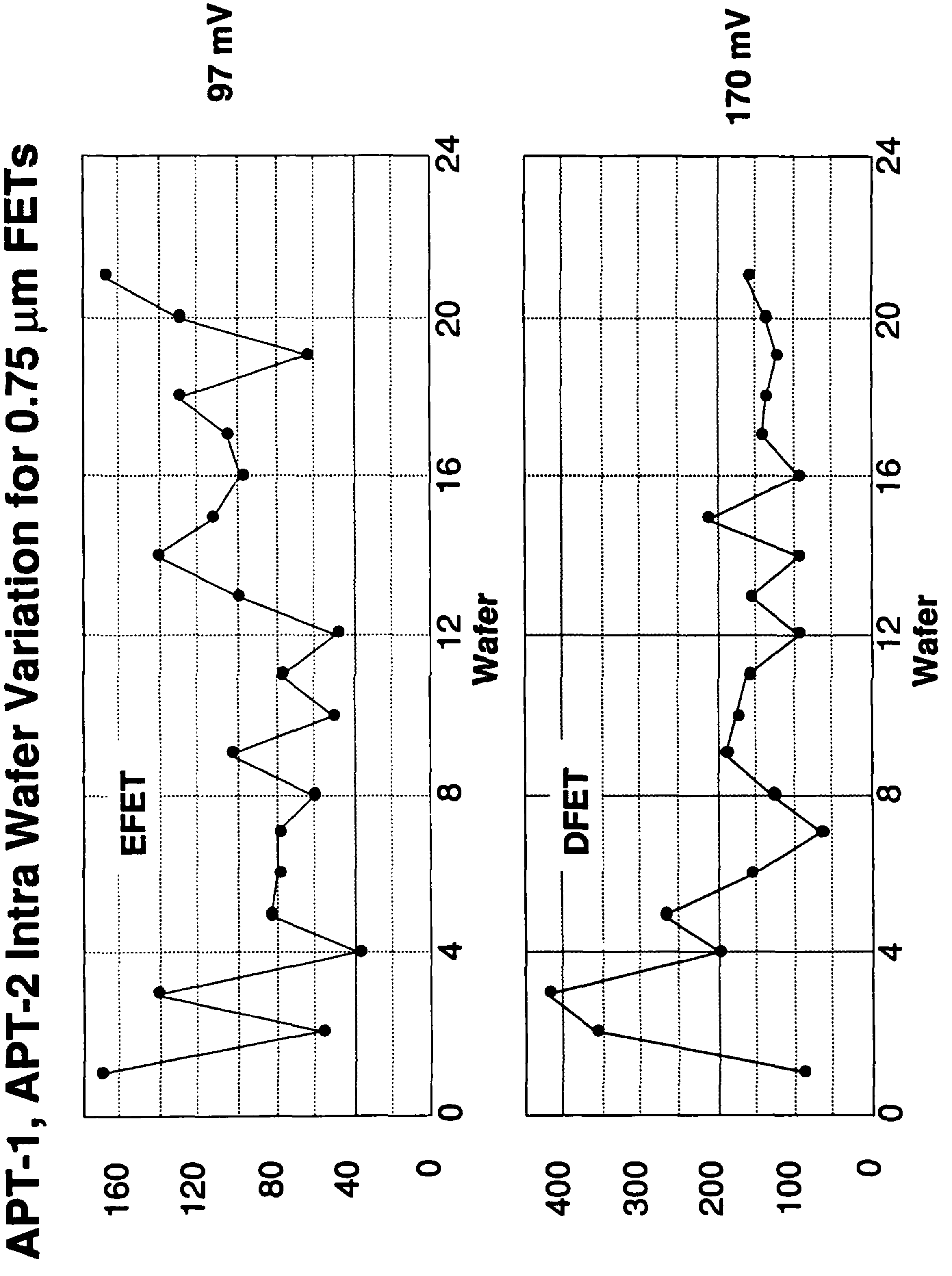
Planarized Dielectric over Gate and Ohmic Metal

Figure 20.



EFET and DFET Threshold Variations for 0.75 μm Gate Lengths in Advanced Technology

Figure 21.



Intrawafer Standard Deviations of Thresholds for 0.75 µm Gate Lengths in Advanced Technology

Figure 22.

lots, and data for aluminum are taken from 10 wafers taken from 2 PT-Y lots. For comparison, we also present 1988 data from PT-X. The results are shown in Figure 23. The Baseline 2.0 µm gold process shows substantial improvement from 1988 to 1989. In comparison to 1989 2.0 µm gold, the 1.5 µm gold has somewhat lower yields for vias and serpentines, and slightly higher yields for crossovers. The product of the three yields is 10% less for 1.5 µm compared to 2.0 µm. No catastrophic lots were observed with 1.5 µm gold using liftoff. However, this technology is expected to be difficult to control in production.

Compared to 1.5 µm gold, 1.5 µm aluminum has higher yield for vias due to better metal coverage into the vias. On the other hand, crossover and serpentine yields are lower due to incomplete removal of aluminum from the troughs described above. In its present form, 1.5 µm aluminum has a 38% lower yield than 1.5 µm gold, but we expect much higher yield when planarization is integrated into the process.

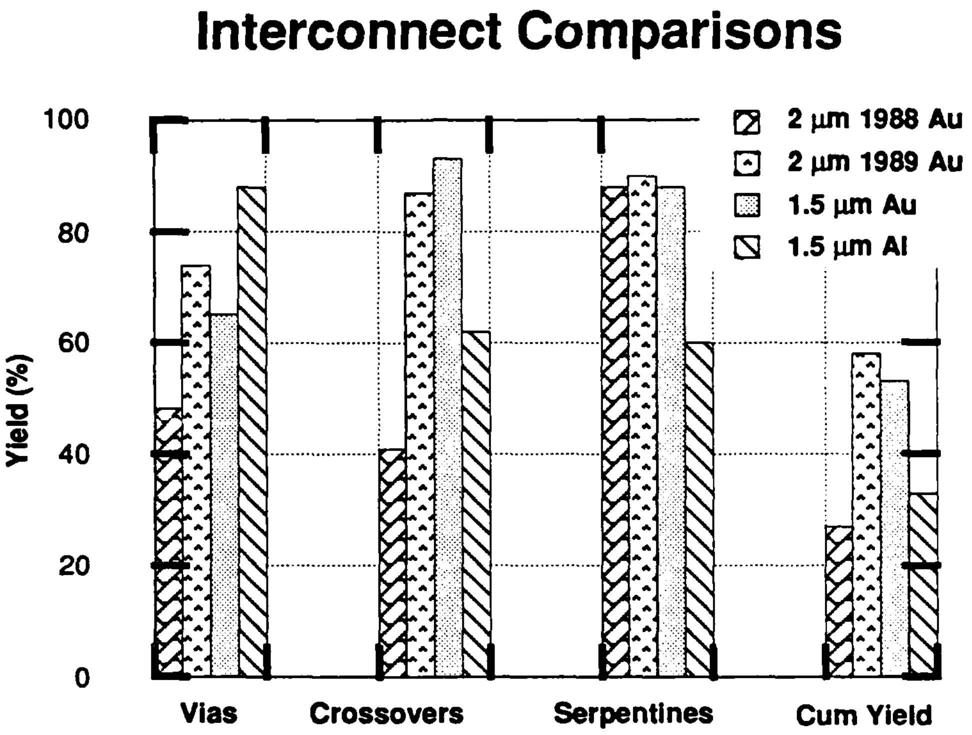
Multiplier Circuit Performance

We tested circuit performance of the Advanced Technology by redesigning the PT-2L Standard Cell 8x8 Multiplier for the Advanced Technology. We named the mask set APT-2. As shown in Figure 24, each reticle field contains four sites:

- Site 1: A direct copy of the PT-2L Multiplier using 2.0 µm design rules
- Site 2: A linear shrink of all components of the PT-2L multiplier to test scaling effects. In Site 2, a feature is 75% of the size in Site 1.
- Site 3: Like Site 4 (the standard Advanced Technology site), except that the FETs were packed as closely as possible, sometimes sharing the same isolation area.
- Site 4: The standard Advanced Technology design using 1.5 µm lines and spaces.

We demonstrated circuit performance using the Advanced Technology design rules with gold metallization and 0.75 µm gates (except for Site 1, which uses 1.0 µm gates). Aluminum metallization was also attempted, but the lots were fabricated before the barrier metal process was fully developed, and they all failed due to gold/aluminum interactions. Because 1.0 µm gates give different FET thresholds than 0.75 µm gates, Site 1 failed to function.

For the required 400 MHz operation with 15 - 20 gate delays, we require operation at 125 ps/gate. Of 312 multipliers tested, 26 worked at 125 ps/gate or faster. Four circuits repeatably ran at 90 ps/gate at close to the required power supply voltage. For the functioning sites, circuit performance is given in Table 13.



	Baseline		Advanced	
	Au PTX	Au PTY	Au	Al
Via Yield*	48%	74%	65%	88%
Crossover Yield*	41%	87%	93%	62%
Serpentine Yield**	88%	90%	88%	60%
Cumulative Yield	17%	58%	53%	33%
Via Do (cm-2)	17.8	7.2	20.1	5.3
Crossover Do	22	3.5	2.7	21
Serpentine Do	8.2	8.6	18.8	75

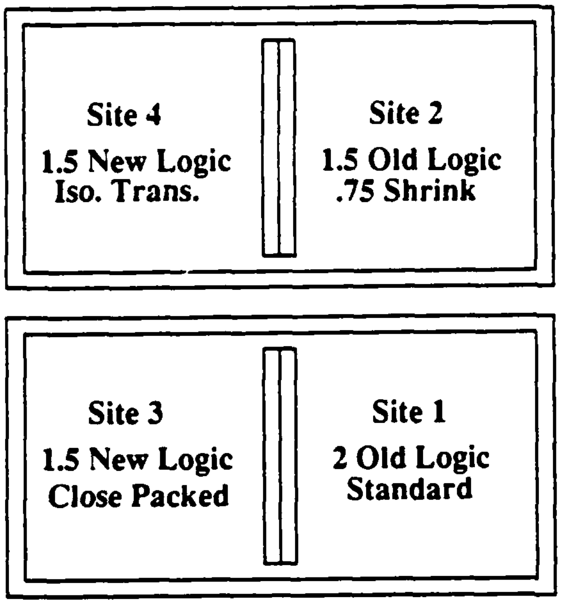
*** Yield for 250,000 via (crossover) testers**

**** Yield for 19 cm of metal - metal runners at minimum space**

Interconnect Yields for 1.5 and 2.0 µm Gold and Aluminum

Figure 23.

APT - 2 Features

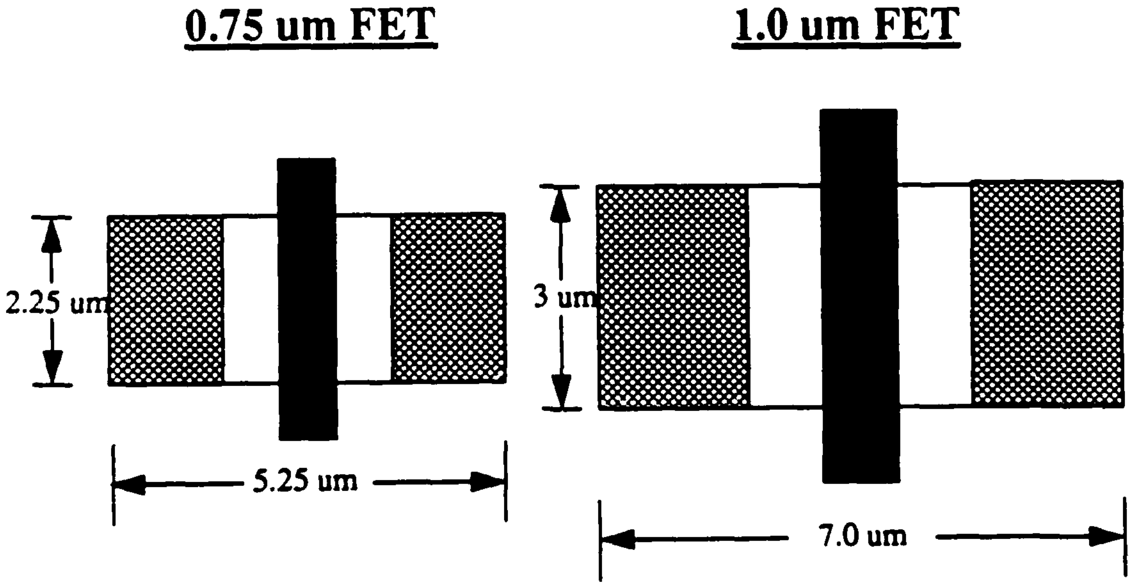

Site 4
1.5 New Logic
Iso. Trans.
Site 2
1.5 Old Logic
.75 Shrink
Site 3
1.5 New Logic
Close Packed
Site 1
2 Old Logic
Standard

Site 1: Original PT-2L 8x8 Multiplier
2.0 um design rules

Site 2: 75% shrink of the PT-2L 8x8
Multiplier → 44% area shrink

Site 3: 1.5 um design rules, E-SFFL Logic,
dense cell layout → 40% area shrink

Site 4: 1.5 um design rules, E-SFFL Logic,
loose cell layout with isolated
transistors → 30% area shrink


0.75 um FET
1.0 um FET
2.25 um
5.25 um
3 um
7.0 um

Layout of APT-2 Test Circuits

Figure 24.

Table 13 — APT-2 YIELDS

Site	Functional	Speed	I/O	Average Current
2	12%	6%	0%	0.561 A
3	24%	11%	8%	0.447 A
4	17%	8%	4%	0.482 A

Functional: passed test vectors at some I/O, speed, and V_{DD}
Speed: faster than 125 ps/gate at some I/O and V_{DD}
I/O: functioned at V_{DD}=2.0 V, V_{ih}<1.0 V, V_{il}>0.3 V, for any speed

These tested devices all came from two wafers, and there was noticeable variation in performance for different areas in the wafers. For example, chips from the tops of the wafers drew twice the current of chips from the bottom. Also, while all input buffers in these three sites were the same, there was considerable I/O performance variation. This makes it hard to draw specific conclusions, but some general trends are clear. First, Site 2 (the linear, or "dumb," shrink) did not perform well. Apparently the design rules must be followed more closely. Second, despite the appearance of Table 13, Site 4 performs better than Site 3. No devices simultaneously meet speed, power supply, and I/O specifications, but Site 4 has the most sites with better performance. We therefore conclude that appropriately separated FETs with proper isolation lead to the best performance.

Extrapolation of Circuit Yield

The objective of the Advanced Technology is to achieve both suitable performance and a predicted 3% DC functional yield. As described above, we developed this process along parallel paths. Along one path, we developed an aluminum metallization process. Simultaneously, along the other path, we used gold interconnects (with 1.5 μm lines and spaces) to demonstrate circuit performance.

For vias, serpentines, and crossovers, we showed above that 1.5 μm gold interconnects have a 10% lower yield than 2.0 μm gold interconnects. In addition to that, there are two ways to look at the circuit yield.

- Table 13 shows a 17% functional yield for Site 4. This compares with a 27% yield achieved with the PT-2L version of the same circuit. This is a 37% yield reduction for the Advanced Technology.
- Alternatively, we can compare PCM yields for the two technologies in comparable time periods. Then the Baseline Technology has a 28% PCM yield, while the Advanced Technology has a 6.4% PCM yield. This is a 77% yield reduction for the Advanced Technology.

Multiplying the interconnect yield times the circuit yield, we find that the Advanced Technology has a 21 - 57% yield compared to the Baseline Technology. That is, when the Baseline Technology achieves a 10% yield, the Advanced Technology is expected to have a 2.1 - 5.7% yield. This compares to the 3% goal.

We showed above that the via, serpentine, and crossover yield is 38% lower for 1.5 μm aluminum than for 1.5 μm gold. However, that yield was obtained with an aluminum process that omitted the desired planarization step. When planarization is integrated into the aluminum metal process, we expected a yield comparable to or better than gold.

4.6 Packaging Support and Assembly (T. S. Freese, R. S. Moyer, R. B. Crispell)

The most recent package/circuit assignment summary is provided in Table 14.

Status of Assembly Issues Presented in the Previous Technical Report

Plastic Carriers for Interamics 64/88 Packages

Plastic carriers were ordered to contain and protect package leads during handling and shipping for the Interamics 64/88 package. These carriers have been received and are in limited use. However, the plastic carriers cannot be made from an ESD dissipating material without an additional investment of $20K for a new mold. Rather than make this investment, the testing group has been made aware of proper ESD handling procedures. Potential ESD damage of circuits can occur if the carriers are used without proper ESD precautions. Therefore, carrier usage is limited to the testing group for straightening and preserving package leads during testing.

Wirebonding High I/O Count Dice

Circuits with I/O counts exceeding 200 are now being produced by the Pilot Line. They present a challenge to the wire bond assembly due to the number of wires and, in part, to the use of packages which are not customized to the circuits. We are taking steps to allow either manual or automatic wirebonding. Each process has its advantages and disadvantages.

Manual wirebonding has the advantage of the human operator's ability to tailor wire paths to the circuit and package. Disadvantages include high cost and, of course, human errors. We are labeling the I/O pads on the circuits to help in locating and identifying the I/Os. Automatic wirebonding is more reproducible, but it cannot tailor each wire path. Prior to assembly of actual devices, mechanical samples of dice suitable for wirebonding are being used to evaluate the best wirebonding process for that device.

New Assembly Issue and Resolution

The TriQuint packages have provisions for mounting external by-pass capacitors to the package. AT&T is attaching them using conductive epoxy. On a recent lot of packaged ALU circuits, power and ground planes were found to be shorted together during testing. The devices were returned to Reading, where we discovered epoxy

DARPA PILOT LINE III
PACKAGE-CIRCUIT ASSIGNMENT SUMMARY

Package Cost @ 100 Quantity	Pitch Z_0	Signal Leads Total Leads	Cavity Size Max Die Size	High Speed Fixture Available	Burn-in Sockets Available	Circuit Reticle Date	Die Size	Signal Count Total I/O	Packages Required for RAD HARD Testing	Packages Required for REL. Testing
Tri-Quint PK-MLC-44-S $65	.050" 50Ω	24 44	.130" SQ .090" SQ	Yes TriQuint	Yes JEDEC	PT-1 11/87	.060" SQ	24 44	40	275 for 256 Bit SRAM
						PT-2M 10/88	.080" SQ	16 44		
Interamics 64/88 $170	.020" 50Ω	64 88	.250" SQ .210" SQ	Yes In House	2/89 Azimuth Elect.	PT-2L 6/88	.204" SQ	64 88	60	275 for 4K SRAM
						4K SRAM 9/89	.216" SQ	~36 88		
						1K Cell Array 4/89	.212" SQ	64 88		
TriQuint PK-MLC 196-S $180	.025" 50Ω	128 196	.430" SQ .390" SQ	Yes TriQuint	6/89 Yes	Transversal Filter Chip 9/89	.360" SQ	105 173	40	
						Custom ALU 3/89	.292" SQ	120 168		
						Standard Cell ALU 8/89	.292"SQ	120 168		
						32 Bit Floating Point Multiplier 12/89	.360"x.380"	110 160		
NTK/256 pin $50	.020" 58-60Ω	224 256	.560"SQ .520"SQ	No	Yes Yamaichi	Cell Array Casino Test Chip 12/89	.462"SQ	172 236		

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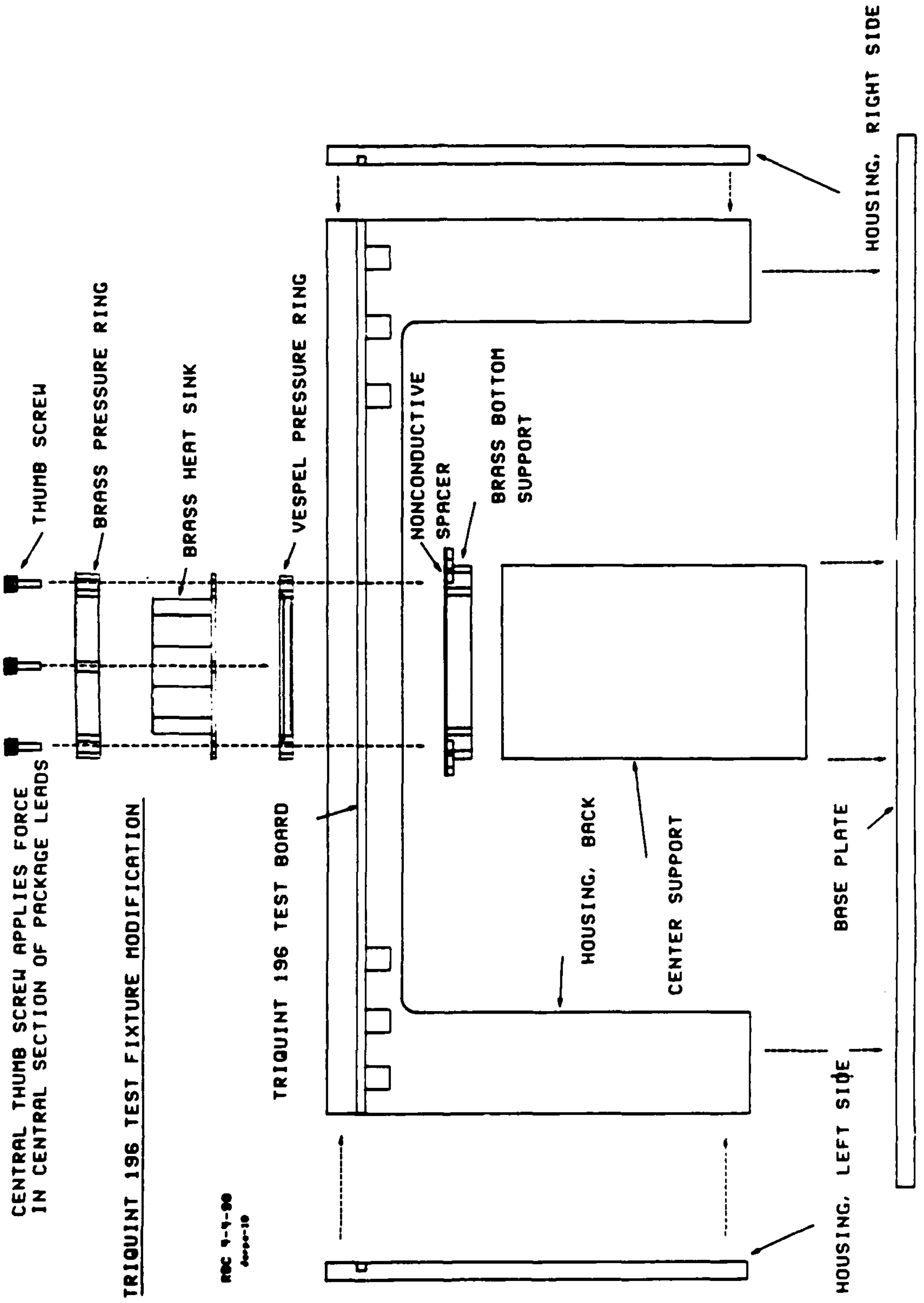
Table 14

used to bond the by-pass capacitors had bridged the bond pads, causing the short circuit. These devices were repaired and retested as deliverable circuits. Assembly operators were alerted to the problem and have reduced the amount of epoxy used to bond the capacitors. In addition, during assembly the packages are checked for possible short circuit occurrence.

Mechanical Improvements to High Speed Test Fixtures

Difficulties were encountered with loading packages into test fixtures and maintaining alignment with all of the package leads. A new package clamping mechanism was designed and fabricated by AT&T, eliminating all of the problems that we were experiencing. A schematic view of the design is shown in Figure 25. This approach was applied to TriQuint 196 lead package testing as well as to Interamics 64/88 package testing. Additionally, the design was communicated to TriQuint so they could incorporate it into their test fixtures if they wish to do so.


TRIQUINT 196 TEST FIXTURE MODIFICATION
CENTRAL THUMB SCREW APPLIES FORCE IN CENTRAL SECTION OF PACKAGE LEADS
THUMB SCREW
BRASS PRESSURE RING
BRASS HEAT SINK
VESPEL PRESSURE RING
TRIQUINT 196 TEST BOARD
NONCONDUCTIVE SPACER
BRASS BOTTOM SUPPORT
HOUSING, BACK
CENTER SUPPORT
BASE PLATE
HOUSING, RIGHT SIDE
HOUSING, LEFT SIDE
RBC 9-4-90

Clamping Mechanism for TriQuint 196 Package Testing

Figure 25.

5. RELIABILITY AND QUALITY

5.1 Radiation Hardness Testing (S. B. Witmer, M. Spector)

Total Dose Testing

Total dose radiation testing was performed on Advanced Process Technology discrete FETs and ring oscillators. The devices were exposed to gamma radiation up to 1×10^8rad(GaAs) from a Co^{60} source. The average change in threshold voltage after 1×10^8rad(GaAs) was 18 mV and 22 mV in EFETs and DFETs, respectively. A 10% decrease in oscillation frequency in ring oscillators was also observed at 1×10^8rad(GaAs) (see Figure 26). The results are comparable to the Baseline Technology total dose results.

Transient Ionizing Dose Testing

Transient ionizing dose testing was performed on Advanced Process Technology (APT) FETs and ring oscillators from two different lots. The results were lot dependent; but, in general, the reduction of the drain to source resistance due to the 30ns radiation pulse with the gate voltage biased at $V_{gs}<V_{th}$ was larger in APT FETs than in Baseline FETs.

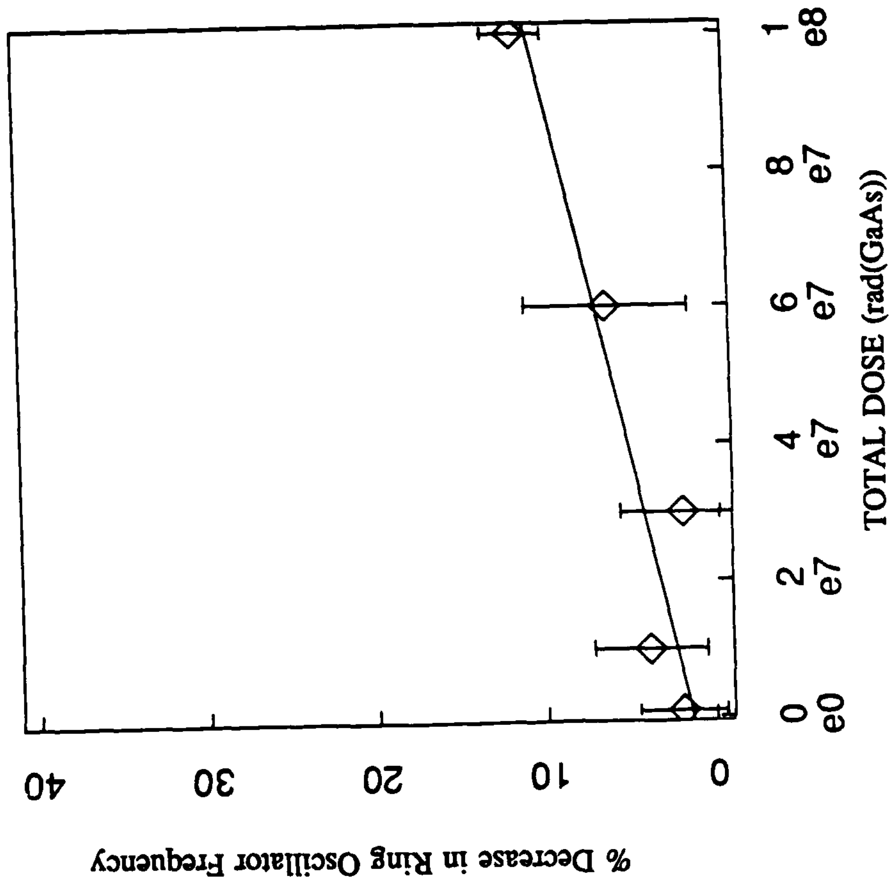
APT ring oscillators stopped oscillating at dose rates of approximately 5×10^8rad(GaAs)/sec with recovery times in milliseconds. These results differ greatly from the Baseline Technology ring oscillators where oscillations stopped at approximately 5×10^9rad(GaAs)/sec with prompt recovery times of less than 50 ns.

Single Event Upset Testing

The 256 bit PT-2M SRAM was tested for single event upsets at Brookhaven National Laboratory. The SRAMs were irradiated with the following ions: He, Li, F, I, and Ni, producing linear energy transfers in GaAs ranging from $0.1MeV*cm^2/mg$ to $44MeV*cm^2/mg$. Both static testing, where the SRAM is read only once after the radiation exposure, and dynamic testing, where the SRAM is read and corrected continuously during the exposure, were used to evaluate the SRAMs. In both the static and dynamic test modes, the LET threshold was about $0.2MeV*cm^2/mg$ and $0.35MeV*cm^2/mg$ for the standard and rad-hard designs, respectively. At an LET value of $44MeV*cm^2/mg$ using Ni, the upset cross-sections per cell were approximately $2.25\times10^{-6}cm^2$ and $1.22\times10^{-6}cm^2$ for the standard and rad-hard SRAMs, respectively (see Figure 27). Row failures (multiple bits in a row fail simultaneously) occurred frequently during the dynamic and static testing when irradiated with Ni ($LET=44MEV*cm^2/mg$ at 30° tilt), indicating that multiple upsets occur from one ion hit.

5.2 Reliability Testing (P. F. Thompson)

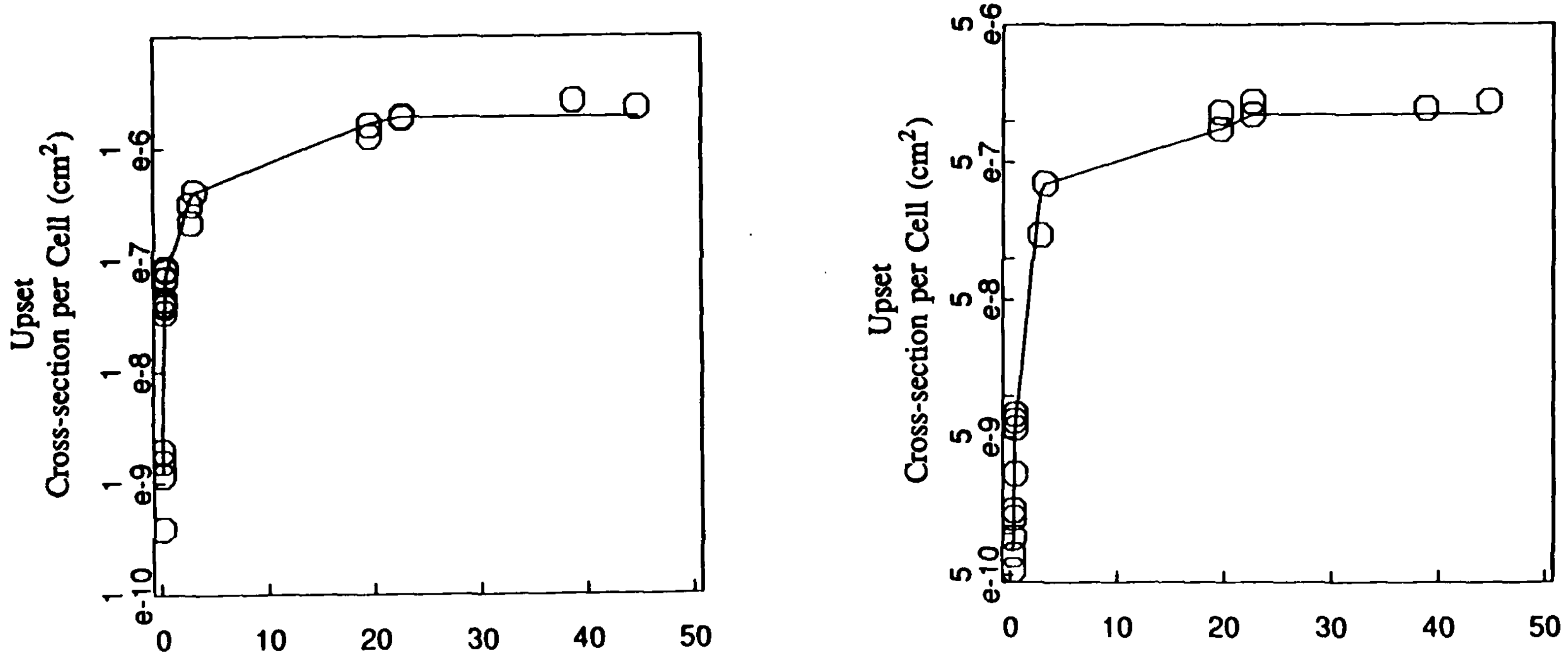
Reliability activities occurred in two areas this reporting period: PT-2M HTOB (thermal aging and high temperature operating bias) and accelerated electromigration



Total Dose Irradiation of Advanced Technology Ring Oscillator

Figure 26.

SINGLE EVENT UPSET:256-BIT GaAs SRAM



Device 32882-4171:STANDARD DESIGN

Device 32882-5162:RAD-HARD

Single Event Upset in PT-2M Memory

Figure 27.

testing in support of the APT program.

PT-2M devices (4 each at 150°C, 175°C, 200°C and controls) are being thermally aged (no bias). Through 1000 hours, no significant changes or trends in parameter values or device performance has occurred. Aging is continuing, with the next parametric test scheduled for 1750 hours. The PT-2M thermal aging is the first long-term reliability study of AT&T's digital SARGIC technology, and good stability to thermal effects is indicated.

PT-2M devices (30 each at 150°C, 175°C, 200°C and 10 controls) are also undergoing HTOB (High Temperature Operating Bias) testing. Through 64 hours, no significant device changes have occurred, reinforcing the thermal aging results.

There are no results yet from Advanced Technology accelerated electromigration.

5.3 Process Control Implementation (P. F. Thompson)

During the last six months, use of Statistical Process Control (SPC) charts has been integrated into a total quality management (TQM) plan. As a result, process control implementation has become more structured, consistent and widespread.

The weekly SPC issues meeting instituted during the last period has been continued and expanded. The total set of charts is now analyzed, rather than a subset of wafer fab only. During this period, we have decreased the number of out of range points from an average of approximately 25% to less than 5% on a weekly basis, and have achieved our first weeks with no out of range points.

The number of quality improvement teams has been increased during the last six months. There are several types of teams ranging from functional teams that deal with one process block (metals, photoresist, etc.) to a team for the entire GaAs business unit. The number of functional teams has increased to nine, covering MBE through final test. All teams meet on a regular basis (typically every 2-3 weeks), and have identified suppliers and customers for their block, plus key metrics for monitoring and improving their processes.

Use and understanding of SPC continues to grow. Virtually all operations have control charts in place, or are currently starting charts. A study of all existing charts is underway to assure that utility, and not just quantity, of charts is improved. A training session on construction and interpretation of SPC charts was held for all management and engineering. Shop personnel are also receiving instruction through the functional team leaders and in-house quality consultants.

Statistical design of experiments has recently been used to help improve process control. Designed experimentation has been successfully used to both solve problems and increase process robustness.